

EDS MAYA Classification Report for 839873.

1. 371/37.7 Total=8 ORs=6 XRs=2
 Class 371 ERROR DETECTION/CORRECTION AND FAULT
 DETECTION/RECOVERY
 Sub 30 DIGITAL DATA ERROR CORRECTION
 Sub 37.01 .Forward correction by block code
 Sub 37.7 ..Error correcting code with additional error
 detection code (e.g., cyclic redundancy character,
 parity)
2. 371/37.12 Total=5 ORs=3 XRs=2
 Class 371 ERROR DETECTION/CORRECTION AND FAULT
 DETECTION/RECOVERY
 Sub 30 DIGITAL DATA ERROR CORRECTION
 Sub 37.01 .Forward correction by block code
 Sub 37.07 ..Code based on generator polynomial
 Sub 37.12 ...Syndrome computed
3. 395/182.04 Total=5 ORs=4 XRs=1
 Class 395 INFORMATION PROCESSING SYSTEM ORGANIZATION
 Sub 180 RELIABILITY AND AVAILABILITY
 Sub 181 .Fault recovery
 Sub 182.01 ..By masking or reconfiguration
 Sub 182.03 ...Of memory or peripheral subsystem
 Sub 182.04 Redundant stored data accessed (e.g., duplicated
 data, error correction coded data, or other
 parity-type data)
4. 371/3 Total=4 ORs=2 XRs=2
 Class 371 ERROR DETECTION/CORRECTION AND FAULT
 DETECTION/RECOVERY
 Sub 3 TESTING OF ERROR-CHECK SYSTEM
5. 371/37.4 Total=4 ORs=3 XRs=1
 Class 371 ERROR DETECTION/CORRECTION AND FAULT
 DETECTION/RECOVERY
 Sub 30 DIGITAL DATA ERROR CORRECTION
 Sub 37.01 .Forward correction by block code
 Sub 37.4 ..Double encoding codes (e.g., product,
 concatenated)
6. 371/37.6 Total=4 ORs=1 XRs=3
 Class 371 ERROR DETECTION/CORRECTION AND FAULT
 DETECTION/RECOVERY
 Sub 30 DIGITAL DATA ERROR CORRECTION
 Sub 37.01 .Forward correction by block code
 Sub 37.6 ..Parallel generation of check bits
7. 371/40.11 Total=4 ORs=3 XRs=1
 Class 371 ERROR DETECTION/CORRECTION AND FAULT
 DETECTION/RECOVERY
 Sub 30 DIGITAL DATA ERROR CORRECTION
 Sub 37.01 .Forward correction by block code
 Sub 40.11 ..Memory access

8.	371/40.2	Total=4	ORs=1	XR=3
	Class 371	ERROR DETECTION/CORRECTION AND FAULT		
		DETECTION/RECOVERY		
	Sub 30	DIGITAL DATA ERROR CORRECTION		
	Sub 37.01	.Forward correction by block code		
	Sub 40.11	..Memory access		
	Sub 40.2	...Error correct and restore		
9.	371/40.3	Total=4	ORs=2	XR=2
	Class 371	ERROR DETECTION/CORRECTION AND FAULT		
		DETECTION/RECOVERY		
	Sub 30	DIGITAL DATA ERROR CORRECTION		
	Sub 37.01	.Forward correction by block code		
	Sub 40.11	..Memory access		
	Sub 40.3	...Error pointer		
10.	371/40.4	Total=4	ORs=0	XR=4
	Class 371	ERROR DETECTION/CORRECTION AND FAULT		
		DETECTION/RECOVERY		
	Sub 30	DIGITAL DATA ERROR CORRECTION		
	Sub 37.01	.Forward correction by block code		
	Sub 40.11	..Memory access		
	Sub 40.4	...Check bits stored in separable area of memory		

?show files;ds

File 351:DERWENT WPI 1963-1999/UD=9911;UP=9911;UM=9911

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File 344:Chinese Patents ABS Apr 1985-1999/Jan

(c) 1999 European Patent Office

File 347:JAPIO Oct 1976-1998/Nov.(UPDATED 990312)

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Set	Items	Description
S1	7718	MC=(U21-A06? OR W01-A01B?) <i>Error Correction / Detection</i>
S2	8779	IC=H03M-013
S3	40718	BI()DIRECTION? OR BIDIRECTION? OR TWO(2W)DIRECTION? OR "2"- ()DIRECTION? OR MORE()THAN()ONE()DIRECTION? OR DUAL(2W)DIRECT- ION? OR PLURALITY(2W)DIRECTION?
S4	16686	ERROR? ?(3N) (DETECT? AND CORRECT?)
S5	41	S1 AND S3
S6	33	S2 AND S3
S7	96	S3 AND S4
S8	31463	PROGRAMMABLE
S9	2	S5:S7 AND S8
S10	230	S3(5N)PROGRAM?
S11	175	S4(5N)PROGRAM?
S12	0	(S1:S2 OR S4) AND S10
S13	1	S3 AND S11
S14	143	S5:S7
S15	24	S14 AND (BUS OR EDIT OR BUFFER)
S16	3	S14 AND (THIRD OR THREE OR TRI? OR TRIPLE?) (2W)BUS
S17	4	S13 OR S16
S18	20	S15 NOT S17
S19	4	S13 OR S17
S20	20	S18 NOT S19
?		

?t19/4/all

19/4/1 (Item 1 from file: 351)

DIALOG(R) File 351:DERWENT WPI

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IM- *Image available*

AA- 90-126705/199017|

XR- <XRPX> N90-098127|

TI- **Error detecting** system for triply redundant information bus - has three selectors each comparing two inputs with its output and also using inter selector comparison|

PA- THOMSON CSF (CSFC)|

NC- 001|

NP- 001|

PN- FR 2636151 A 19900309 FR 8811496 A 19880902 199017 B

|

AN- <LOCAL> FR 8811496 A 19880902|

AN- <PR> FR 8811496 A 19880902|

AB- <BASIC> FR 2636151 A

An **error detection and correction** system for data flowing on a triply redundant parallel information bus uses three selectors (1,2,3) which "vote". The **three** incoming bus (11,12,13) and the **three** outgoing bus (51, 52, 53) are respectively connected to the three selectors and internal state bus circuits (B13, B12, B23) provide communication between the selectors. Information for external equipment is transmitted through further state bus (EE1, EE2, EE3).

Each of the three selectors is additionally connected to the incoming bus of one of the other two selectors and also to the outgoing bus of the other of these two selectors. These connections allow each selector to compare its own and one other input with its output and to resolve any inequalities by comparison with other selectors thus identifying any errors or faults.

USE/ADVANTAGE - For calculators with improved reliability. Selector faults as well as information **errors** are **detected** and the system is **bidirectional** . (21pp Dwg.No.1/4)|

DE- <TITLE TERMS> ERROR; DETECT; SYSTEM; TRIPLE; REDUNDANT; INFORMATION; BUS; THREE; SELECT; COMPARE; TWO; INPUT; OUTPUT; INTER; SELECT; COMPARE

|

DC- T01|

IC- <ADDITIONAL> G06F-011/16|

MC- <EPI> T01-G03|

FS- EPI||

19/4/2 (Item 2 from file: 351)

DIALOG(R) File 351:DERWENT WPI

(c)1999 Derwent Info Ltd. All rts. reserv.

AA- 89-339659/198946|

XR- <XRPX> N89-258552|

TI- Error tolerant microprocessor - detects and **corrects** random soft **errors** during **program** execution occurring in memory during each cycle|

PA- GALAXY MICROSYST (GALA-N)|

AU- <INVENTORS> FOSDICK R E|

NC- 001|

NP- 001|

PN- US 4866718 A 19890912 198946 B

|

AN- <PR> US 8789221 A 19870825|

AB- <BASIC> US 4866718 A

the microprocessor utilises a bit serial architecture and single error correction double error detection techniques that automatically detect and correct soft errors occurring in its internal memory elements during each word cycle. The microprocessor automatically detects and corrects soft errors during each word cycle. The error detection and correction is transparent to the external microprocessor

interface.

The microprocessor also uses a multi-level hierarchal structure. The architecture utilises a set of multi-stage serial data shift registers (55) to store data and instruction words (bits) in bit serial fashion. A set of multi-stage shift registers (59) is used to store error code word bits (58) corresponding to a parallel set of bits (57). (Multi-bit error Correctable Word or ECW) in the data shift registers. The shift registers may be parallel or serial. An error code generator and comparator circuit shown as block (60) is used to generate and compare error codes based on well known single error correction double error detection (SECDED) coding techniques. A select code circuit (54) coupled to a **bidirectional** data bus (53) communicates with the data shift registers. Function units (5052) or any standard arithmetic logic unit may be used to perform basic arithmetic and logic operations. A control circuit

(100) is used to control the operations of the central processing unit.

ADVANTAGE - Maintains high instruction execution throughput. (12pp Dwg.No.1/5)

DE- <TITLE TERMS> ERROR; TOLERATE; MICROPROCESSOR; DETECT; CORRECT; RANDOM; SOFT; ERROR; PROGRAM; EXECUTE; OCCUR; MEMORY; CYCLE|

DC- T01|

IC- <ADDITIONAL> G06F-011/00|

MC- <EPI> T01-G; T01-G01|

FS- EPI||

19/4/3 (Item 3 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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AA- 89-070377/198910|

XR- <XRPX> N89-053716|

TI- Dual rail processors with error checking at single rail interfaces - has shared resource devices coupled to processors for receiving data from output instructions from processors simultaneously|

PA- DIGITAL EQUIP CORP (DIGI)|

AU- <INVENTORS> BISSETT T D; BRUCKERT W F; RIEGELHAUPT N H; RIEGELHAUP N H|

NC- 006|

NP- 005|

PN- EP 306209 A 19890308 EP 88307854 A 19880824 198910 B

PN- US 4907228 A 19900306 US 8793584 A 19870904 199016

PN- CA 1299756 C 19920428 CA 576411 A 19880902 G06F-011/16 199222

PN- EP 306209 B1 19950621 EP 88307854 A 19880824 G06F-011/16 199529

PN- DE 3854025 G 19950727 DE 3854025 A 19880824 G06F-011/16 199535

<AN> EP 88307854 A 19880824|

AN- <LOCAL> EP 88307854 A 19880824; US 8793584 A 19870904; CA 576411 A 19880902; EP 88307854 A 19880824; DE 3854025 A 19880824; EP 88307854 A 19880824|

AN- <PR> US 8793584 A 19870904|

CT- A3...9039; DE 3328405; EP 120384; EP 77154; No-SR.Pub|

FD- EP 306209 A

<DS> (Regional): FR GB IT

FD- EP 306209 B1

<DS> (Regional): DE FR GB IT

FD- DE 3854025 G Based on EP 306209|

LA- EP 306209(E<PG> 14); EP 306209(E<PG> 84)|

DS- <REGIONAL> FR; GB; IT; DE|

AB- <BASIC> EP 306209 A

The dual processor computer system with error checking includes one processing system for executing a series of instructions including output instructions. A second processing system executes the series of instructions independently of an in synchronism with the first processing system. Shared resource devices are coupled to the processing systems for receiving data from output instructions from the processing systems simultaneously.

Error checking devices are located downstream of the shared resource for checking the data received from the processing systems

only following a write operation into the shared resource.

Dwg.1/28|

AB- <EP> EP 306209 B

A fault tolerant computing system (10) comprising: a first dual processor computer system (20) including: a first central processing unit (40) executing a series of instructions including output instructions containing data to be written into a first designated system element (60); a second central processing unit (50) executing said series of instructions independently of and in synchronism with said first central processing unit; a first data bus (46) coupled to said first central processing unit (40) for receiving said data from said first central processing unit; a second data bus (56) coupled to said second central processing unit (50) for receiving said data from said second central processing unit; first shared resource means (60), coupled to said first and second data buses (46,56) for serving as a first designated system element for selected ones of said output instructions executed by said first and second central processing units, for simultaneously receiving said data from said first and second central processing units and for recording the data contained in said ones of said selected output instructions, said first shared resource means including a first memory (600) for storing said data, first data selection means (70) for transmitting data from only one of said first and second processing units to said first memory; and first error checking means (70,75) coupled to said first and second data buses (46,56) for checking said data on said first and second data buses to **detect and correct errors** only following a read operation of said first memory; a second dual processor computer system (20') including: a third central processing unit (40') executing said series of instructions independently of and in synchronism with said third central processing unit; a **third data bus** (46') coupled to said third central processing unit (40') for receiving said data from said third central processing unit; a fourth data bus (56') coupled to said fourth central processing unit (50') for receiving said data from said fourth central processing unit; second shared resource means (60') coupled to said third and fourth data buses (46',56) for serving as a second designated system element for selected ones of said output instructions executed by said third and fourth central processing units, for simultaneously receiving said data from said third and fourth central processing units and for recording said data contained in said selected output instructions, said second shared resource means including a second memory (600') for storing said data, second data selection means (70') for transmitting data from only one of said third and fourth central processing units to said second memory; and second error checking means (70',75'), coupled to said third and fourth data buses (46',56'), for checking said data on said third and fourth data buses to **detect and correct errors** only during a read of said second memory; and cross-link communication means (25) coupled between said first and second dual processor computer systems (20,20') for providing **bi-directional** communication between said first and second dual processor computer systems and for maintaining the operation of said first and second dual processor computer systems (20,20') in lock step synchronism in the absence of errors.

(Dwg.1/28|

AB- <US> US 4907228 A

The dual processor computer system has a processing system for executing a series of instructions including output instructions containing data to be written into a designated system element. A second processing system executes the series of instructions independently of an in synch. with the first processing system. A shared resource is coupled to the two processing systems. The shared resource serves as a designated element for selected ones of output instructions executed by the two processing systems and for recording the data contained in the selected ones of the output instructions. The shared resource receives data from the two processing systems simultaneously.

An error checking circuit coupled to the shared resource and to the two processing systems. The data received by said share resource from said first and second processing systems is checked for **errors**.

The **error** checking **corrects** the **errors** only when the selected ones of the output instructions are executed by the two processing systems to write data into the shared resource.

ADVANTAGE - Error checking capability|

DE- <TITLE TERMS> DUAL; RAIL; PROCESSOR; ERROR; CHECK; SINGLE; RAIL;
INTERFACE; SHARE; RESOURCE; DEVICE; COUPLE; PROCESSOR; RECEIVE; DATA;
OUTPUT; INSTRUCTION; PROCESSOR; SIMULTANEOUS|

DC- T01|

IC- <MAIN> G06F-011/16|

IC- <ADDITIONAL> G06F-011/00|

MC- <EPI> T01-G03; T01-J02|

FS- EPI||

19/4/4 (Item 4 from file: 351)

DIALOG(R) File 351:DERWENT WPI

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AA- 84-147803/198424|

DX- <RELATED> 89-095253; 89-116276|

XR- <XRPX> N84-109899|

TI- High speed, compact digital data processing system - has serial
input-output unit providing communication with soft console and another
unit for communication with bulk memory devices|

PA- DATA GENERAL CORP (DATG)|

AU- <INVENTORS> ANDERSON W; BURNS K; EPSTEIN D I; GUYER J M; HUMMEL M D;
KEATING D L; NORMOYLE K B; VERES J E|

NC- 012|

NP- 019|

PN- EP 110613 A 19840613 EP 83306958 A 19831115 198424 B

PN- AU 8320139 A 19840524 198428

PN- BR 8306259 A 19840731 198438

PN- CA 1198221 A 19851217 198604

PN- CA 1198223 A 19851217 198604

PN- US 4569018 A 19860204 US 82441967 A 19821115 198608

PN- CA 1204216 A 19860506 198623

PN- CA 1204217 A 19860506 198623

PN- CA 1204218 A 19860506 198623

PN- CA 1204220 A 19860506 198623

PN- US 4591972 A 19860527 US 82441969 A 19821115 198624

PN- US 4597041 A 19860624 US 82441839 A 19821115 198628

PN- CA 1206267 A 19860617 198629

PN- IL 70230 A 19880429 198827

PN- IL 82688 A 19880429 198827

PN- IL 82689 A 19880429 198827

PN- EP 110613 B 19910710 199128

PN- DE 3382334 G 19910814 199134

PN- JP 8016388 A 19960119 JP 83213888 A 19831114 G06F-009/26 199613

<AN> JP 91287423 A 19831114|

AN- <LOCAL> EP 83306958 A 19831115; US 82441967 A 19821115; US 82441969 A
19821115; US 82441839 A 19821115; JP 83213888 A 19831114; JP 91287423 A
19831114|

AN- <PR> US 82441969 A 19821115; US 82441836 A 19821115; US 82441837 A
19821115; US 82441838 A 19821115; US 82441839 A 19821115; US 82441966 A
19821115; US 82441967 A 19821115|

CT- 3.Jnl.Ref; A3...8703; EP 39227; No-SR.Pub|

FD- EP 110613 A

<DS> (Regional): DE FR GB IT NL SE

FD- EP 110613 B

<DS> (Regional): DE FR GB IT NL SE

FD- JP 8016388 A Div ex JP 83213888|

LA- EP 110613(E<PG> 114); JP 8016388(31)|

DS- <REGIONAL> DE; FR; GB; IT; NL; SE|

AB- <BASIC> EP 110613 A

A processor provides addresses to a memory on an address bus. Data and instructions pass between the memory and the processor via a data bus. The processor houses an internal data-bus which provides data to a central processor which performs the arithmetical and logical

operations commanded by the user program instructions.

The output of the CPU passes to another internal bus. A memory data buffer is used to transfer data from the internal data-bus to the main memory and from the latter to the internal output bus. A nibble shifter and a scratch pad memory are connected between the internal buses. A control unit operates the system by microprogram. A microsequencer has a permanent store for a kernel microcode and a writable memory for further microcodes which can be entered via the main memory to adapt the system to a specific instruction set. A memory control unit performs **error detection** and **correction** and other memory related operations.

Dwg.0/71

AB- <EP> EP 110613 B

A data processing system comprising processor means (PU 106) responsive to instructions for processing the data and for providing physical memory addresses for reading the data from and writing the data to a main memory (102) which is responsive to the memory addresses for storing and providing the data and instructions, and memory bus means (MAD 108, MDA 110) for conducting the memory addresses, data and instructions between the processor means and the main memory means, the processor means (PU 106) comprising first and second buses (YBUS 124, D BUS 112), input/output means (MDB 132) connected between the memory bus means (MAD 108, MDA 110) and the first bus for input and the second bus for output, CPU means (122) having an input connected from the second bus and an output connected to the first bus, and processor memory means (SPAD 128) connected between the first bus (YBUS 124) and the second bus (D BUS 112), the processor memory (SPAD 128) having scratch pad memory means for storing CPU data, and for storing and providing address information for relating user program logical addresses of corresponding storage locations in the main memory (102), characterised in that the processor memory means (SPAD 128) comprises - third and fourth buses (LAR BUS 132, SPAD BUS 134) an addressing buffer (LARR 136) connected from the first bus (YBUS 124) to the **third bus** (LAR BUS 132), - a **bidirectional** buffer (SPADB 152) connected between the second bus (DBUS 112) and the fourth bus, and that the scratch pad memory (SPADM 129) having a **bidirectional** data port connected from and to the fourth bus (SPAD BUS 134) and an addressing input (AD) and - scratch pad addressing means (SPAM 144) having an addressing output connected to the scratch pad memory addressing input (AD) and a first address input connected from the **third bus** (LAR BUS 132). (34pp)|

AB- <US> US 4597041 A

A memory stores the data to be processed and the instructions for directing operations of the system.

An I/O unit is connected between an external terminal providing directing commands and an external memory, coupling being made via a bus.

A microcode control provides sequences of micro-instructions. A kernel microcode memory responds to certain first instructions and commands for storing and providing corresp. micro-instruction sequences for controlling certain first operations.

A writable microcode memory responds to certain second instructions and commands.

ADVANTAGE - Enhances operating speed, efficiency and system capabilities.

(26pp)

US 4591972 A

A register is connected to an instruction receiver and a state receiver and is responsive to a sequence control internal microcode control for receiving and storing an initial address of a presently selected one of the microinstruction sequences. A microcode program counter is connected to the register and is responsive to the sequence control internal microcode control for receiving the initial address.

The counter provides successive addresses of the presently selected one of the microinstruction sequences. An address multiplexer is connected to the register the counter and the microcode control for providing the addresses to the microcode memory. A microcode state save device including microcode state register is connected to the sequence control.

(26pp)

US 4569018 A

The data processing system includes a memory means for storing and providing data and instructions.

The memory comprises storage locations, each responsive to a physical address.

The instructions direct operation of the data processing system where each instruction comprises an operation code for specifying an operation to be performed by the data processing system.

Each instruction comprises Data specifiers specify certain data on which operations are to be performed.

The data specifiers include memory address specifiers for specifying locations of the certain data in the memory.

The memory address specifiers include physical addresses for directly addressing certain of the storage locations of the memory to obtain the data and logical addresses from which physical addresses may be determined.

USE - High speed, compact, data processing systems.

(26pp)|

DE- <TITLE TERMS> HIGH; SPEED; COMPACT; DIGITAL; DATA; PROCESS; SYSTEM;
SERIAL; INPUT; OUTPUT; UNIT; COMMUNICATE; SOFT; CONSOLE; UNIT;
COMMUNICATE; BULK; MEMORY; DEVICE|

DC- T01|

IC- <MAIN> G06F-009/26|

IC- <ADDITIONAL> G06F-009/22; G06F-012/10; G06F-013/00; G11C-009/06|

MC- <EPI> T01-E; T01-F; T01-H; T01-J|

FS- EPI||

?

?t20/5/all

20/5/1 (Item 1 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011621694 **Image available**
WPI Acc No: 98-038822/199804
XRPX Acc No: N98-031294

Bus system for connection of various apparatus - has apparatus management unit to give approval for apparatus to use bi-directional bus and control of bi-directional bus is performed

Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 9293048	A	19971111	JP 96131345	A	19960427	G06F-013/36	199804 B

Priority Applications (No Type Date): JP 96131345 A 19960427

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 9293048	A		6			

Abstract (Basic): JP 9293048 A

The system has **bi-directional bus** (20) connected to various apparatuses (30). An apparatus management unit (10) monitors the apparatus and according to its requirement.

The apparatus management unit allows the apparatus to use the **bi-directional bus**. Only after approval by the apparatus management unit the apparatus controls the **bi-directional bus**.

ADVANTAGE - Prevents hindrance to operation of normal apparatus. Prevents malfunctioning of apparatus.

Dwg.1/2

Title Terms: **BUS** ; SYSTEM; CONNECT; VARIOUS; APPARATUS; APPARATUS; MANAGEMENT; UNIT; APPROVE; APPARATUS; BI; DIRECTION; **BUS** ; CONTROL; BI; DIRECTION; **BUS** ; PERFORMANCE

Derwent Class: T01; U21

International Patent Class (Main): G06F-013/36

International Patent Class (Additional): G06F-011/20; G06F-011/30; G06F-013/00

File Segment: EPI

20/5/2 (Item 2 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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011416927 **Image available**
WPI Acc No: 97-394834/199737
XRPX Acc No: N97-328551

Sensor and actuator bus system for automation system - has transformation units each converting transmitted signals into number sequence for increased transmission reliability

Patent Assignee: LEUZE ELECTRONIC GMBH & CO (LEUZ-N)
Inventor: BAUDER F; KELLER R; MUELLER B; STARK K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
DE 19614654	C1	19970821	DE 1014654	A	19960413		199737 B

Priority Applications (No Type Date): DE 1014654 A 19960413

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
DE 19614654	C1		8			

Abstract (Basic): DE 19614654 C

The **bus** system has **bus** lines (4) coupled to the interface modules (6) of the sensors and actuators (2) for **bidirection** exchange

of signals, with a control unit (3) for cyclic interrogation of the sensors and/or actuators, coupled to a signal evaluation device (5). the interface module of at least one sensor and/or actuator is preceded by transformation unit (7) , with a second transformation unit (8) inserted between the control unit and the evaluation device, each converting the transmitted signals into a number sequence.

ADVANTAGE - Increased transmission reliability, and error immunity.

Dwg.1/2

Title Terms: SENSE; ACTUATE; BUS ; SYSTEM; AUTOMATIC; SYSTEM; TRANSFORM; UNIT; CONVERT; TRANSMIT; SIGNAL; NUMBER; SEQUENCE; INCREASE; TRANSMISSION ; RELIABILITY

Derwent Class: S02; T06; U21; W01; W02; W05

International Patent Class (Main): H04L-001/08

International Patent Class (Additional): G01D-005/00; G05B-009/02;

G08C-019/28; H03M-013/00 ; H04L-012/40

File Segment: EPI

20/5/3 (Item 3 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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011327260 **Image available**

WPI Acc No: 97-305164/199728

XRPX Acc No: N97-252708

Bidirectional data communication system with encoded digital image transmitting function - includes image decoder that decodes image data based on updated data received by reception side from retransmission frame determination unit

Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 9116904	A	19970502	JP 95269769	A	19951018	H04N-007/30	199728 B

Priority Applications (No Type Date): JP 95269769 A 19951018

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 9116904	A		11			

Abstract (Basic): JP 9116904 A

The system includes an image encoder (1) that orderly outputs image data arranged in each block provided with number of bits. The image of each block is compressed. The block data and compressed image are classified for every number of bits, providing a recognition number in a frame. A frame structure (2) combines each frame in the order of the recognition number, comprising a transmitted frame data. The frame data is received by a receiving buffer (6) from a transmitting buffer (3), and is divided to block data. The compressed image data is decoded in a reproduction image data, reproducing the image.

The recognition number of the frame containing the block is determined, if the transmitted block is in accord with the block currently recorded. A receiver (200) has a retransmission frame determination unit (5) that transmits a resending signal containing the determined frame to a reception side. The reception side receives the retransmitted signal. An image decoder (7) decodes the image based on the received updated data.

ADVANTAGE - Communicates image data without reducing through-put since transmission of error detection code to reception side is cancelled.

Dwg.1/7

Title Terms: BIDIRECTIONAL ; DATA; COMMUNICATE; SYSTEM; ENCODE; DIGITAL; IMAGE; TRANSMIT; FUNCTION; IMAGE; DECODE; DECODE; IMAGE; DATA; BASED; UPDATE; DATA; RECEIVE; RECEPTION; SIDE; RETRANSMISSION; FRAME; DETERMINE; UNIT

Index Terms/Additional Words: ARQ

Derwent Class: U21; W01; W02; W04

International Patent Class (Main): H04N-007/30

International Patent Class (Additional): H03M-013/00 ; H04L-001/18;
H04N-001/41
File Segment: EPI

20/5/4 (Item 4 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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010642378 **Image available**

WPI Acc No: 96-139332/199614

XRPX Acc No: N96-116773

Stuck faults detection for branch instruction condition signals, for detecting faults in digital computer systems - uses data processing system contg. programmable microprocessor and multiple VLSI gate arrays connected by bidirectional bus, with branch condition obtained from storage location on VLSI gate array

Patent Assignee: UNISYS CORP (BURS)

Inventor: BYERS L L; DE SUBIJANA J M; MICHAELSON W A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5495598	A	19960227	US 93173598	A	19931223	G06F-011/00	199614 B

Priority Applications (No Type Date): US 93173598 A 19931223

Patent Details:

Patent	Kind	Lan	Pg	Filing	Notes	Application	Patent
US 5495598	A		26				

Abstract (Basic): US 5495598 A

The processor generates request to external device to return the state of the designator, sending signal from external device to processor acknowledging receipt of the request, reading the state of the designator by external device, and sending true condition signal pulse representing the state of the designator with a first continuous predetermined width from the external device to the processor over the signal line. The VLSI gate array executes asynchronous and external to the microprocessor. The branch condition is fetched and evaluated in parallel with fetching of branch target address and incrementing of the program counter.

The microprocessor changes instruction sequence control depending on the results of the branch condition evaluation. The branch condition is sent to the microprocessor as a signal pulse for a specified duration at a particular time, rather than by changing the level of the signal, thereby allowing communication of the branch condition over only one signal line but still providing for detection of faults in the VLSI gate array or faults inherent in the signal line.

ADVANTAGE - Provides capability to change instruction sequence control depending on value resident in device external to microprocessor.

Dwg.7/12

Title Terms: STICK; FAULT; DETECT; BRANCH; INSTRUCTION; CONDITION; SIGNAL; DETECT; FAULT; DIGITAL; COMPUTER; SYSTEM; DATA; PROCESS; SYSTEM; CONTAIN; PROGRAM; MICROPROCESSOR; MULTIPLE; VLSI; GATE; ARRAY; CONNECT; **BIDIRECTIONAL ; BUS ; BRANCH; CONDITION; OBTAIN; STORAGE; LOCATE; VLSI; GATE; ARRAY**

Derwent Class: T01; U21

International Patent Class (Main): G06F-011/00

International Patent Class (Additional): H03M-013/00

File Segment: EPI

20/5/5 (Item 5 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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010592539 **Image available**

WPI Acc No: 96-089492/199610

XRPX Acc No: N96-074967

Electronic instrument for TV receivers for controlling e.g. picture-in-picture processing etc - has control device coupled to at least one peripheral unit via communication bus for bi-directional communication with peripheral unit

Patent Assignee: THOMSON CONSUMER ELECTRONICS INC (THOH)

Inventor: BROWNING D M; EDDE G A; LANDIS M D; BROWNING M D

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
GB 2292238	A	19960214	GB 9515105	A	19950724	G06F-001/24	199610 B
US 5528749	A	19960618	US 94286472	A	19940805	G06F-011/34	199630
JP 8153012	A	19960611	JP 95229561	A	19950804	G06F-011/00	199633
CN 1119305	A	19960327	CN 95109226	A	19950804	G06F-011/00	199744
SG 46948	A1	19980320	SG 951063	A	19950804	G06F-011/34	199818

Priority Applications (No Type Date): US 94286472 A 19940805

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
GB 2292238	A		11			
US 5528749	A		5			
JP 8153012	A		6			

Abstract (Basic): GB 2292238 A

The instrument includes a peripheral unit for processing signals. A control device is coupled to the peripheral unit via a communications bus for bidirectional communication with the peripheral unit. A nonvolatile memory device is coupled to the control device, for storing data indicative of the operational status of the peripheral unit.

A power supply device is coupled to the control device, and coupled to the peripheral unit for supplying power to the peripheral unit. The control device determines the operational status data of the peripheral unit via communication over the communications bus . E.g. on detection of an error condition,

the

control device writes the data indicative of operational status to the memory circuit.

USE/ADVANTAGE - In bus controlled TV receivers. Provision for automatic error correction .

Dwg.1/2

Title Terms: ELECTRONIC; INSTRUMENT; TELEVISION; RECEIVE; CONTROL; PICTURE; PICTURE; PROCESS; CONTROL; DEVICE; COUPLE; ONE; PERIPHERAL; UNIT; COMMUNICATE; BUS ; BI; DIRECTION; COMMUNICATE; PERIPHERAL; UNIT

Derwent Class: T01; U24; W03

International Patent Class (Main): G06F-001/24; G06F-011/00; G06F-011/34

International Patent Class (Additional): G06F-001/26

File Segment: EPI

20/5/6 (Item 6 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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010146032 **Image available**

WPI Acc No: 95-047284/199507

XRPX Acc No: N95-037501

Decoder for digital communication - incorporates memory to record error correction code by direct interface with error correction circuit, monitored by control signals from control circuit

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 6326692	A	19941125	JP 93112742	A	19930514	H04L-001/00	199507 B

Priority Applications (No Type Date): JP 93112742 A 19930514

Patent Details:

Abstract (Basic): JP 6326692 A

The decoder consists of a memory (33) which is interfaced with a **error correction** circuit (32), a control circuit (35) and a frame synchronisation detection circuit (34). A monitoring circuit (31) is connected to the memory through the **error correction** circuit. The monitoring circuit is also directly connected to the control circuit to facilitate **bi-directional** flow of control signal.

A memory stores and retrieves data after **error correction** on a first in first out basis. The characteristic properties of input signal with a synchronising pattern are found in the detection circuit under control by the initiation of control circuit. If they match, then the signal details are recorded in the data **buffer**. The detection is constantly monitored for any variations between various frames being transmitted. Hence **error correcting** codes is decoded for multiple frames of data being transmitted.

ADVANTAGE - Facilitates high speed operation. Obtains miniaturisation.

Dwg.3/7

Title Terms: DECODE; DIGITAL; COMMUNICATE; INCORPORATE; MEMORY; RECORD; ERROR; CORRECT; CODE; DIRECT; INTERFACE; ERROR; CORRECT; CIRCUIT; MONITOR ; CONTROL; SIGNAL; CONTROL; CIRCUIT

Derwent Class: W01

International Patent Class (Main): H04L-001/00

International Patent Class (Additional): H03M-013/00 ; H04L-007/08

File Segment: EPI

20/5/7 (Item 7 from file: 351)

DIALOG(R) File 351:DERWENT WPI

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010123297 **Image available**

WPI Acc No: 95-024548/199504

Related WPI Acc No: 89-350111

XRPX Acc No: N95-019062

Transparent latch circuit for buffering and parity checking data communicated between two data buses - includes number of bidirectional bit buffer circuits and data receiver, latch and driver between buses, with parity generation at latch stage

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: BLAND P M; DEAN M E; GAUDENZI G J; KRAMER K G; TEMPEST S L

Number of Countries: 004 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 630112	A2	19941221	EP 89480053	A	19890411	H03K-019/082	199504 B
			EP 94113671	A	19890411		
EP 630112	A3	19951122	EP 94113671	A	19890411		199618 B

Priority Applications (No Type Date): US 88198961 A 19880526

Cited Patents: No-SR.Pub; 1.Jnl.Ref; EP 154330; US 4528465

Patent Details:

Patent Kind Lan Pg Filing Notes Application Patent

EP 630112 A2 E 14 Related to EP 89480053

Designated States (Regional): DE FR GB IT

EP 630112 A3 Related to EP 344081

Abstract (Basic): EP 630112 A

The latch circuit includes a number of **bidirectional** bit **buffer** circuits. Each circuit includes a data path comprising a data receiver (57), latch (58) and driver (60) connected in series between the two data buses (52,54) to be buffered and checked. A second data path comprises a data receiver (66), a latch (64) and a driver (62) connected in series between the two data buses.

A control circuit controls the drivers to selectively place the output of the drivers in an active driving or high impedance state and

to control the data latches to selectively latch or pass through data. A parity generating circuit (68) is connected at the output of the latch in the first data path of each of the **buffer** circuits for generating a parity bit responsive to the data at the output of these latches. A transparent driver circuit with a phase splitter is provided for increasing the speed of the circuit.

USE/ADVANTAGE - In signal processing circuits. Transparent latch circuit for generating and verifying parity as function of data held in latch. Enables latching of data without imposing any significant delay between input and output devices. Increased operating speed.

Dwg. 5A/5

Title Terms: TRANSPARENT; LATCH; CIRCUIT; **BUFFER** ; PARITY; CHECK; DATA; COMMUNICATE; TWO; DATA; **BUS** ; NUMBER; **BIDIRECTIONAL** ; BIT; **BUFFER** ; CIRCUIT; DATA; RECEIVE; LATCH; DRIVE; **BUS** ; PARITY; GENERATE; LATCH; STAGE

Derwent Class: U21; W01

International Patent Class (Main): H03K-019/082

International Patent Class (Additional): G06F-011/10; G06F-013/40; H03K-019/00; **H03M-013/00**

File Segment: EPI

20/5/8 (Item 8 from file: 351)

DIALOG(R) File 351:DERWENT WPI

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009315440 **Image available**

WPI Acc No: 93-008904/199301

XRPX Acc No: N93-006760

Fault-tolerant corrector and detector IC device - includes field programmable gate arrays and output circuitry connecting memory registers and data path for high-speed data processing

Patent Assignee: US DEPT ENERGY (USAT); AMERICAN TELEPHONE & TELEGRAPH CO (AMTT)

Inventor: ANDALEON D D; NAPOLITANO L M; REDINBO G R; SHREEVE W O

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 7599606	A	19921201	US 90599606	A	19901018	G06F-000/00	199301 B
US 5291496	A	19940301	US 90599606	A	19901018	G06F-011/10	199409

Priority Applications (No Type Date): US 90599606 A 19901018

Patent Details:

Patent	Kind	Lan	Pg	Filing	Notes	Application	Patent
US 7599606	A		48				
US 5291496	A		18				

Abstract (Basic): US 7599606 A

The internally fault-tolerant data **error detection** and **correction** integrated circuit device (10) includes field programmable gate arrays and circuitry to output register contents to a data path. The device functions as a **bidirectional** data **buffer** between a 32-bit data processor and the remainder of a data processing system and provides a 32-bit data having a relatively short eight bits of data-protecting parity. The 32-bits of data by eight bits of parity is partitioned into eight 4-bit nibbles and two 4-bit nibbles, respectively. For data flowing towards the processor the data and parity nibbles are checked in parallel and in a single operation employing a dual orthogonal basis technique.

Any one of ten (eight data, two parity) nibbles are correctable if erroneous, or two different erroneous nibbles are detectable. For data flowing away from the processor the approp. parity nibble values are calculated and transmitted to the system along with the data. The device regenerates parity values for data flowing in either direction and compares regenerated to generated parity with a totally self-checking equality checker.

USE/ADVANTAGE - For **error detection** chip. Self-validating, detects and indicates internal failure. Detection using relatively short parity code, with max. error performance bound for linear codes

for 32-bit datum.

Dwg.1/5

Title Terms: FAULT; TOLERATE; CORRECT; DETECT; IC; DEVICE; FIELD; PROGRAM;
GATE; ARRAY; OUTPUT; CIRCUIT; CONNECT; MEMORY; REGISTER; DATA; PATH; HIGH
; SPEED; DATA; PROCESS

Index Terms/Additional Words: INTEGRATED; CIRCUIT

Derwent Class: T01

International Patent Class (Main): G06F-011/10

International Patent Class (Additional): G06F-011/16; H03M-013/00

File Segment: EPI

20/5/9 (Item 9 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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009308042 **Image available**

WPI Acc No: 93-001478/199301

XRPX Acc No: N93-000987

**Memory subsystem using faulty chips for computer memory - uses 6-bit
error detection and correction to correct one faulty bit in each
word**

Patent Assignee: SGS THOMSON MICROELTRN INC (SGSA)

Inventor: RAASCH R W

Number of Countries: 004 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 520676	A2	19921230	EP 92305540	A	19920617	G06F-011/10	199301 B
EP 520676	A3	19931110	EP 92305540	A	19920617	G06F-011/10	199512

Priority Applications (No Type Date): US 91722937 A 19910628

Cited Patents: No-SR.Pub; US 3644902; US 3814922

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
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EP 520676	A2	E	6			
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Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 520676 A

The memory subsystem uses memory chips known to have bad bits. The memory subsystem (16) includes a bus data interface (22) and bus control circuits (24) for **bidirectional** memory access. Bus addresses (26) are decoded and applied to the memory array (28) in they are within its 8 Mbyte address range. Data written to the memory have an additional 6 bits of **error detection and correction** data added, and the 22 bits are written to the memory array.

On reading the memory, the **error** circuits **correct** no more than 1 error bit per word. As only a few words contain a hard error, most words are protected against single bit soft faults.

ADVANTAGE - Provides memory using inexpensive faulty memories and provides better protection.

Dwg.2/3

Title Terms: MEMORY; SUBSYSTEM; FAULT; CHIP; COMPUTER; MEMORY; BIT; ERROR;
DETECT; CORRECT; CORRECT; ONE; FAULT; BIT; WORD

Derwent Class: T01

International Patent Class (Main): G06F-011/10

File Segment: EPI

20/5/10 (Item 10 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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009072943 **Image available**

WPI Acc No: 92-200363/199224

XRPX Acc No: N92-151510

**Multiple microcontroller hard disk drive control architecture - has
independently operating low-level and interface controllers and arbiter
controller responsive to data transfer requests for data storage and
retrieval**

Patent Assignee: CONNER PERIPHERALS INC (CONN-N)
 Inventor: CLAY D W; KEELER S M; SANDER C M; SQUIRES J P
 Number of Countries: 016 Number of Patents: 012
 Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
WO 9209036	A1	19920529	WO 91US8061	A	19911029	G06F-013/14	199224 B
EP 556324	A1	19930825	WO 91US8061	A	19911029	G06F-013/14	199334
			EP 92901005	A	19911029		
US 5261058	A	19931109	US 90611141	A	19901109	G06F-013/14	199346
			US 9327614	A	19930305		
US 5274773	A	19931228	US 90611141	A	19901109	G06F-013/14	199401
			US 92997860	A	19921229		
JP 6502267	W	19940310	WO 91US8061	A	19911029	G06F-003/06	199415
			JP 92501844	A	19911029		
US 5412666	A	19950502	US 90611141	A	19901109	G06F-011/10	199523
			US 92997898	A	19921229		
US 5610808	A	19970311	US 90611141	A	19901109	G05B-015/02	199716
			US 92997898	A	19921229		
			US 94315129	A	19940929		
EP 556324	A4	19970312	EP 92901005	A	19920000	G06F-013/14	199729
KR 97703012	A	19970610	WO 91US8061	A	19911029	G06F-009/46	199825
			KR 96706112	A	19961029		
KR 97703013	A	19970610	WO 91US8061	A	19911029	G06F-009/46	199825
			KR 96706113	A	19961029		
KR 97703014	A	19970610	WO 91US8061	A	19911029	G06F-009/46	199825
			KR 96706115	A	19961029		
KR 97703031	A	19970610	WO 91US8061	A	19911029	G11B-021/10	199825
			KR 96706114	A	19961029		

Priority Applications (No Type Date): US 90611141 A 19901109; US 9327614 A 19930305; US 92997860 A 19921229; US 92997898 A 19921229; US 94315129 A 19940929

Cited Patents: US 4371929; US 4371932; US 4949245; US 4979056; US 4987530; US 5072420; WO 9005339

Patent Details:

Patent	Kind	Lan	Pg	Filing	Notes	Application	Patent
WO 9209036	A1	E	62				
					Designated States (National): JP KR		
					Designated States (Regional): AT BE CH DE DK ES	FR GB GR IT LU NL SE	
EP 556324	A1	E	2	Based on		WO 9209036	
					Designated States (Regional): DE FR GB IT NL		
US 5261058	A		25	Cont of	US 90611141		
US 5274773	A		25	Div ex	US 90611141		
JP 6502267	W			Based on		WO 9209036	
US 5412666	A		25	Div ex	US 90611141		
US 5610808	A		26	Div ex	US 90611141		
				Cont of	US 92997898		
				Cont of		US 5412666	
KR 97703012	A			Based on		WO 9209036	
KR 97703013	A			Based on		WO 9209036	
KR 97703014	A			Based on		WO 9209036	
KR 97703031	A			Based on		WO 9209036	

Abstract (Basic): WO 9209036 A

The disk drive architecture (10) controls data transfer between a host processor interface (50) and a magnetic disk (14). A low-level data controller controls the transfer of data between the disk and a data **buffer**. An interface controller (52) controls the transfer of data between the host interface (50) and the data **buffer**.

An arbiter and **buffer** controller (32,34) respond to data transfer requests from the two controllers and arbitrate data storage and retrieval access of the data **buffer**. The low-level and interface controllers operate independently of each other. Consequently, data is transferred **bi-directionally** through data **buffer** at the optimum times for both controllers.

USE/ADVANTAGE - High performance multiprocessor control system for hard disk drives. High access and data transfer speeds. High reliability. Low cost.

Dwg.1/7

Title Terms: MULTIPLE; HARD; DISC; DRIVE; CONTROL; ARCHITECTURE;
INDEPENDENT; OPERATE; INTERFACE; CONTROL; ARBITER; CONTROL; RESPOND; DATA
; TRANSFER; REQUEST; DATA; STORAGE; RETRIEVAL
Derwent Class: T01; T03
International Patent Class (Main): G05B-015/02; G06F-003/06; G06F-009/46;
G06F-011/10; G06F-013/14; G11B-021/10
File Segment: EPI

20/5/11 (Item 11 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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008946350 **Image available**

WPI Acc No: 92-073619/199210

XRPX Acc No: N92-055361

Checksum calculating in data communications - working in parallel with
DMA transfer of data under DMA control between memory and communications
interface

Patent Assignee: HONEYWELL INC (HONE)

Inventor: GONIA P S; HOFF J F

Number of Countries: 006 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 473102	A	19920304	EP 91114329	A	19910827		199210 B
CA 2050099	A	19920301	CA 2050099	A	19910828	H04L-001/00	199224
JP 4358245	A	19921211	JP 91242445	A	19910829	G06F-013/00	199304
EP 473102	A3	19930107	EP 91114329	A	19910827		199345
EP 473102	B1	19951122	EP 91114329	A	19910827	G06F-011/08	199551
DE 69114788	E	19960104	DE 614788	A	19910827	G06F-011/08	199606
			EP 91114329	A	19910827		
US 5500864	A	19960319	US 90574822	A	19900829	G06F-011/10	199617
			US 9376827	A	19930614		

Priority Applications (No Type Date): US 90574822 A 19900829; US 9376827 A
19930614

Cited Patents: NoSR.Pub; 1.Jnl.Ref; JP 63217736; US 3573726; US 4555784

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 473102	A					
				Designated States (Regional): DE FR GB		
EP 473102	B1	E	15			
				Designated States (Regional): DE FR GB		
DE 69114788	E			Based on		EP 473102
US 5500864	A		15	Cont of	US 90574822	

Abstract (Basic): EP 473102 A

The communications system has a host computer (12) connected to a network interface (14) with an attached checksum calculation unit (10). Data for communication is moved to/from the host computer and a network memory (22) under the control of a data flow control unit (18) which generates DMA addresses for both the host memory and the network memory.

During transfers a checksum calculation unit (16) forms check sums of the data transferred in parallel with the transfer and provides the check sums to the host or network memory.

ADVANTAGE - Improves throughput and transmission times.

Dwg.1/6

Title Terms: CALCULATE; DATA; COMMUNICATE; WORK; PARALLEL; DMA; TRANSFER;
DATA; DMA; CONTROL; MEMORY; COMMUNICATE; INTERFACE
Derwent Class: T01; W01
International Patent Class (Main): G06F-011/08; G06F-011/10; G06F-013/00;
H04L-001/00
International Patent Class (Additional): H03M-013/00
File Segment: EPI

20/5/12 (Item 12 from file: 351)

DIALOG(R)File 351:DERWENT WPI
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008821385 **Image available**
WPI Acc No: 91-325398/199144
Related WPI Acc No: 91-281646; 91-281651; 91-353965
XRPX Acc No: N91-249422

Failure tolerant mass storage system - uses disk drives coupled to small buffers and error correction controller coupled to number of X bar switches

Patent Assignee: MICRO TECHNOLOGY INC (MICR-N); SF2 CORP (SFTW-N)
Inventor: GAJJAR K; HENSON L P; IDLEMAN T E; POWERS D T; IDLEMAN T; POWERS D

Number of Countries: 032 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
WO 9115822	A	19911017					199144 B
EP 532514	A1	19930324	EP 91908123	A	19910403	G06F-011/20	199312
			WO 91US2315	A	19910403		
EP 532514	A4	19931006	EP 91908123	A	19910000		199527
EP 532514	B1	19971126	EP 91908123	A	19910403	G06F-011/20	199801
			WO 91US2315	A	19910403		
DE 69128284	E	19980108	DE 628284	A	19910403	G06F-011/20	199807
			EP 91908123	A	19910403		
			WO 91US2315	A	19910403		

Priority Applications (No Type Date): WO 91US2315 A 19910403

Cited Patents: 1.Jnl.Ref; US 3988543; US 4212080; US 4722085; US 4736376;
US 4807183; US 4807184; US 4817035; US 4885741; US 4914656; US 4924458;
EP 294287; EP 319188; EP 369707; US 3634830; US 4024498; US 4775978

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
WO 9115822	A					
Designated States (National): AT AU BB BG BR CA CH DE DK ES FI GB HU JP KP KR LK LU MC MG MW NL NO RO SD SE SU						
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LU NL OA SE						
EP 532514	A1	E		Based on		WO 9115822
Designated States (Regional): DE FR GB IT						
EP 532514	B1	E	34	Based on		WO 9115822
Designated States (Regional): DE FR GB IT						
DE 69128284	E			Based on		EP 532514
				Based on		WO 9115822

Abstract (Basic): WO 9115822 A

The system for storing data comprises a number of memory storage units, and a number of output buffers coupled to the first **bus**. Several multiplexing switch units are individually coupled to each individual memory storage unit by a **bidirectional bus** and to each individual output **buffer** by a **bidirectional bus**. A controller coupled to each multiplexing switch unit controls the multiplexing switch unit to allow data to flow from any selected output **buffer** to any selected memory storage and to flow from any selected memory storage to any output **buffer**. An **error detector** is coupled individually to each switch by the **bus** and is used for **detecting** and **correcting errors** in the data as the data is transmitted in parallel both from the **buffer** to the data storage through the switch unit and from the data storage to the **buffer** via the switch unit.

A controller controls the operation of the **error detector**. The controller is additionally coupled to the data storage unit and the **buffer** to receive the locations of the failed buffers and data storage, which is then electronically decoupled by the **error detector** from the system.

ADVANTAGE - Multiple **buffer** memories can be read from or written to in sequence for transfers on data **bus** to system computer. (50pp
Dwg.No.3/13)

Title Terms: FAIL; TOLERATE; MASS; STORAGE; SYSTEM; DISC; DRIVE; COUPLE;
BUFFER; ERROR; CORRECT; CONTROL; COUPLE; NUMBER; BAR; SWITCH
Derwent Class: T01; W01

International Patent Class (Main): G06F-011/20
International Patent Class (Additional): H04J-015/00
File Segment: EPI

20/5/13 (Item 13 from file: 351)
DIALOG(R) File 351:DERWENT WPI
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008534658 **Image available**
WPI Acc No: 91-038721/199106
XRPX Acc No: N91-029888

Apparatus for decoding and reproducing digital information signal - has error correction circuit which performs error correction of error codes to input data by using error data

Patent Assignee: SONY CORP (SONY)
Inventor: FUKAMI T
Number of Countries: 007 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 411835	A	19910206	EP 90308249	A	19900727		199106 B
CA 2022024	A	19910130					199116
JP 3062624	A	19910318	JP 89197827	A	19890729		199117
EP 411835	A3	19920115	EP 90308249	A	19900727		199321
EP 411835	B1	19950517	EP 90308249	A	19900727	G11B-020/18	199524
DE 69019432	E	19950622	DE 619432	A	19900727	G11B-020/18	199530
			EP 90308249	A	19900727		
US 5430741	A	19950704	US 90556446	A	19900724	G11B-020/18	199532
			US 9396362	A	19930722		
ES 2072396	T3	19950716	EP 90308249	A	19900727	G11B-020/18	199535

Priority Applications (No Type Date): JP 89197827 A 19890729
Cited Patents: NoSR.Pub; 1.Jnl.Ref; EP 105499; EP 140381; EP 232133; WO 8809966

Patent Details:

Patent	Kind	Lan	Pg	Filing	Notes	Application	Patent
EP 411835	A						
					Designated States (Regional): DE ES FR GB		
EP 411835	B1	E	19				
					Designated States (Regional): DE ES FR GB		
DE 69019432	E			Based on			EP 411835
US 5430741	A		15	Cont of		US 90556446	
ES 2072396	T3			Based on			EP 411835

Abstract (Basic): EP 411835 A

The appts. has a number of symbols arranged in matrix form. The apparatus comprises a **buffer** RAM (40) for the input data and an **error detection** circuit (36) for **detecting** an **error** of the input data based on the first **error correction** code and for generating error data of the first **error correction** code.

Another **buffer** RAM (40) writes the generated **error** data. An **error correction** circuit (41) sequentially performs **error corrections** of the first and second **error correction** codes to the input data by using the generated data of the first **error correction** code.

USE/ADVANTAGE - Digital audio or video recording. **Error correction** capability improved and power consumption reduced. (20pp Dwg.No.5/8)

Title Terms: APPARATUS; DECODE; REPRODUCE; DIGITAL; INFORMATION; SIGNAL; ERROR; CORRECT; CIRCUIT; PERFORMANCE; ERROR; CORRECT; ERROR; CODE; INPUT; DATA; ERROR; DATA

Derwent Class: T03; W04

International Patent Class (Additional): G11B-020/18; H03M-013/00

File Segment: EPI

20/5/14 (Item 14 from file: 351)
DIALOG(R) File 351:DERWENT WPI

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008296435 **Image available**

WPI Acc No: 90-183436/199024

XRPX Acc No: N90-142546

Semiconductor dynamic buffer memory device - includes data exchange cycles shaper and address buffer register

Patent Assignee: KOLGANOV V A (KOLG-I)

Inventor: GUTERMAN I Y A; KOLGANOV V A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
SU 1525744	A	19891130	SU 4273290	A	19870630		199024 B

Priority Applications (No Type Date): SU 4273290 A 19870630

Abstract (Basic): SU 1525744 A

The **buffer** store is designed to give better fidelity of stored data and now includes a data exchange cycles shaper and an address **buffer** register, input-output control unit, data **buffer** register, first (13) and second (14) **bidirectional** switches units, first (15) and second (16) units for **detection** and **correction** of **errors**, control signal shaper (17), data register (18) and data corrections control unit (19) all incorporated into each unit for storage and processing of data (4,5).

USE - Computer engineering, i.e. **buffer** memory devices.

Bul.44/30.11.89. (12pp Dwg.No.2/8)

Title Terms: SEMICONDUCTOR; DYNAMIC; **BUFFER** ; MEMORY; DEVICE; DATA; EXCHANGE; CYCLE; SHAPE; ADDRESS; **BUFFER** ; REGISTER

Derwent Class: T01

International Patent Class (Additional): G11C-011/34

File Segment: EPI

20/5/15 (Item 15 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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008084999 **Image available**

WPI Acc No: 89-350111/198948

Related WPI Acc No: 95-024548

XRPX Acc No: N89-266328

Bidirectional buffer with latch and parity capability - has parity generating circuit with transparent and driver circuit with phase splitter

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: BLAND P M; DEAN M E; GAUDENZI G J; KRAMER K G; TEMPEST S L;

KRMAER K G

Number of Countries: 017 Number of Patents: 012

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 344081	A	19891129	EP 89480053	A	19890411		198948 B
BR 8902376	A	19900116					199008
CN 1037981	A	19891213					199038
US 5107507	A	19920421	US 88198961	A	19880526		199219
US 5173619	A	19921222	US 88198961	A	19880526	H03K-019/177	199302
			US 91740757	A	19910805		
KR 9210553	B1	19921205	KR 895485	A	19890426	G06F-013/40	199414
EP 344081	B1	19950816	EP 89480053	A	19890411	G06F-011/10	199537
DE 68923818	E	19950921	DE 623818	A	19890411	G06F-011/10	199543
			EP 89480053	A	19890411		
ES 2075856	T3	19951016	EP 89480053	A	19890411	G06F-011/10	199547
CA 1338155	C	19960312	CA 596778	A	19890414	H04L-005/14	199620
SG 44402	A1	19971219	SG 96189	A	19890411	H03K-019/082	199808
PH 27673	A	19931006	PH 38471	A	19890410	G06F-011/10	199823

Priority Applications (No Type Date): US 88198961 A 19880526; US 91740757 A 19910805

Cited Patents: 3.Jnl.Ref; A3...9118; EP 154330; JP 60043753; JP 61253550;
No-SR.Pub; US 3914628; US 4528465

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 344081	A	E	17			
Designated States (Regional): BE CH DE ES FR GB IT LI NL SE						
US 5107507	A		10			
US 5173619	A		10	Div ex	US 88198961	
EP 344081	B1	E	17			
Designated States (Regional): BE CH DE ES FR GB IT LI NL SE						
DE 68923818	E			Based on		EP 344081
ES 2075856	T3			Based on		EP 344081

Abstract (Basic): EP 344081 A

The circuit for buffering and parity checking digital data communicated between first and second data buses includes a number of directional bit **buffer** circuits. Each of the directional bit **buffer** circuits includes a first data path comprising a data receiver, latch, and driver connected in series between the first and second data buses. A second data patch comprises a data receiver, latch and driver connected in series between the second and first data buses. A control mechanism controls the drivers to selectively place the output of the drivers in an active driving or high impedance state. A parity generating circuit is connected at the output of the latch in the first data path of each of the **bidirectional** bit **buffer** circuits for generating a parity bit responsive to the data at the output of these latches.

A transparent and driver circuit with phase splitter are also provided.

ADVANTAGE -Increased operation speed. No increase in power requirements

Title Terms: **BIDIRECTIONAL** ; **BUFFER** ; LATCH; PARITY; CAPABLE; PARITY; GENERATE; CIRCUIT; TRANSPARENT; DRIVE; CIRCUIT; PHASE; SPLIT

Derwent Class: T01; U21

International Patent Class (Main): G06F-011/10; G06F-013/40; H03K-019/082; H03K-019/177; H04L-005/14

International Patent Class (Additional): H03K-003/037; H03K-003/288; H03K-003/356; H03K-019/00; H03K-019/0175; **H03M-013/00**

File Segment: EPI

20/5/16 (Item 16 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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007919885

WPI Acc No: 89-184997/198925

XRPX Acc No: N89-141253

Code error detector corrector - uses multiplexers to feed data signals over lines to ROM

Patent Assignee: MARTYNENKO E I (MART-I)

Inventor: AVERYANOVA T F; GULKO V T

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
SU 1429324	A	19881007	SU 4105341	A	19860602		198925 B

Priority Applications (No Type Date): SU 4105341 A 19860602

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
SU 1429324	A		5			

Abstract (Basic): SU 1429324 A

The detector has a counter, arithmetic-logic unit and ROM memory to improve the speed of response. If the data signals pass over the **bus** lines (8,16) from the arithmetic-logic unit (5), then the result is fed over the **bus** lines (17,18) to **buffer** memory (7). If the operand signal pass from unit (7) over the buses (17,18), then the tabular result is transmitted over the **bus** lines (8,16) to the unit (5).

The dual -directional travel of the signals over the bus lines (8,16-18) for the ROM (6) is carried out using the multiplexers. Buffer memory (7) receives operationally stores and feeds out data over the dual -directional bus lines (17,18). Buffer memory (4) stores the received word, passing over the dual -directional bus (8).

USE/ADVANTAGE - For electronic digital equipment, part. for automated, telemechanical and computer systems. Bul.37/7.10.88

Dwg.0/0

Title Terms: CODE; ERROR; DETECT; CORRECT; MULTIPLEX; FEED; DATA; SIGNAL; LINE; ROM

Derwent Class: U21

International Patent Class (Additional): H03M-013/00

File Segment: EPI

20/5/17 (Item 17 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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007775565

WPI Acc No: 89-040677/198906

XRPX Acc No: N89-031128

Convolutional code sequential decoder with short re-sync. interval - determines likelihood of each decoded symbol in accordance with algorithm and causes symbols to be read from buffer when likelihood is low

Patent Assignee: NEC CORP (NIDE)

Inventor: YAGI T

Number of Countries: 005 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 302511	A	19890208	EP 88112785	A	19880805		198906 B
JP 1132241	A	19890524	JP 88196726	A	19880805		198927
JP 1198846	A	19890810	JP 88264822	A	19881019		198938
EP 302511	B1	19931229	EP 88112785	A	19880805	H03M-013/12	199401
DE 3886615	G	19940210	DE 3886615	A	19880805	H03M-013/12	199407
			EP 88112785	A	19880805		
US 5642369	A	19970624	US 88229416	A	19880808	H03M-013/12	199731
			US 91737547	A	19910730		
			US 94328088	A	19941024		
US 5710785	A	19980120	US 88229416	A	19880808	H03M-013/12	199810
			US 91737547	A	19910730		
			US 95428795	A	19950424		

Priority Applications (No Type Date): JP 87265643 A 19871020; JP 87197682 A 19870807; JP 88196726 A 19880805

Cited Patents: 1.Jnl.Ref; A3...9028; EP 139511; No-SR.Pub; US 3665396; US 3872432; US 4539684; US 4583078; US 45239684

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 302511	A	E	14			
Designated States (Regional): DE FR GB						
EP 302511	B1	E	15			
Designated States (Regional): DE FR GB						
DE 3886615	G			Based on		EP 302511
US 5642369	A		9	CIP of	US 88229416	
				CIP of	US 91737547	
US 5710785	A		15	CIP of	US 88229416	
				Cont of	US 91737547	

Abstract (Basic): EP 302511 A

The decoder has two buffer storage sections and a decoder coupled to the buffers for receiving a symbol supplied bidirectionally from the second buffer and decoding the supplied symbol in synchronism with a clock pulse cooccurring at a rate higher than said transmission rate. An address device stores the received convolutinally coded symbols into the first buffer at the transmission rate, reading symbols out of the first buffer into the decoder and storing symbols

decoded by the decoder into the second **buffer** . A controller determines the likelihood of each symbol decoded by the decoder in accordance, with a predetermined likelihood algorithm. This causes the address device to read decoded symbols in a backward direction out of the second **buffer** into the decoder when the determination results in a low likelihood value.

An overflow condition of the first **buffer** is detected when a predetermined number of locations are filled with the received symbols and the address device reads symbols out of the first **buffer** into the decoder starting with a symbol spaced by k symbols from a most recently received symbol and causes the decoder to shift the sync timing by one clock interval.

1/6

Title Terms: CONVOLUTE; CODE; SEQUENCE; DECODE; SHORT; SYNCHRONOUS;
INTERVAL; DETERMINE; DECODE; SYMBOL; ACCORD; ALGORITHM; CAUSE; SYMBOL;
READ; **BUFFER** ; LOW

Derwent Class: U21

International Patent Class (Main): H03M-013/12

International Patent Class (Additional): H03M-013/00 ; H04L-001/00;
H04L-027/22

File Segment: EPI

20/5/18 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

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02614654

MEMORY DEVICE

PUB. NO.: 63-231554 [JP 63231554 A]

PUBLISHED: September 27, 1988 (19880927)

INVENTOR(s): ENMEI FUMIO

ISHIBASHI MUTSUYASU

MATSUURA YASUHIKO

APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)

APPL. NO.: 62-063741 [JP 8763741]

FILED: March 20, 1987 (19870320)

INTL CLASS: [4] G06F-012/16; G06F-011/00

JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1
(INFORMATION PROCESSING -- Arithmetic Sequence Units)

JOURNAL: Section: P, Section No. 818, Vol. 13, No. 35, Pg. 39, January
26, 1989 (19890126)

ABSTRACT

PURPOSE: To delete a memory circuit from a trouble suspected scope by providing a circuit to send writing information to a reading information fetching circuit as reading information.

CONSTITUTION: At the time of writing to a memory circuit 1, a writing control signal 52 comes to be '1', and the contents of a writing data register 24 are sent to the memory circuit 1 through an **error correcting** code generating circuit 23 and a driver 20. Simultaneously, the information on a **bidirectional bus** 60 passes through an **error correcting** circuit 25 through a receiver 21 as reading information 51 and is set to a reading data register 26. Consequently, when an abnormality exists at writing information 50 transferred as the reading information 51, the abnormality is discovered by the **error correcting** circuit 25. When the abnormality is detected, a trouble suspected scope is over the position of circuits 23, 20, 21 and 25, and a comparing inspecting circuit 22 knows the inspecting result, and thus, the normality and abnormality of the circuits 20 and 21 can be separated from other circuit and the stopping of the trouble position can be executed.

20/5/19 (Item 2 from file: 347)

DIALOG(R)File 347:JAPIO

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02505033

ERROR DETECTING AND CORRECTING SYSTEM

PUB. NO.: 63-121933 [JP 63121933 A]
PUBLISHED: May 26, 1988 (19880526)
INVENTOR(s): TSUJIOKA SHIGEO
KOBAYASHI ICHIIJI
SADAMITSU HITOSHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 61-267551 [JP 86267551]
FILED: November 12, 1986 (19861112)
INTL CLASS: [4] G06F-011/10; G06F-011/14; G06F-012/16
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units);
45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 767, Vol. 12, No. 370, Pg. 153,
October 05, 1988 (19881005)

ABSTRACT

PURPOSE: To shorten the access time in case of no error by sending a retry indicating signal to a processor when the **detection** result of an **error detector** indicates a **correctable error** and sending **corrected** data to a **bidirectional data bus** at the time of retry.

CONSTITUTION: Data read out from a memory is sent to a main processor 100, and simultaneously, a syndrome generator 260 generates a syndrome by this data and check bits to **detect** an **error**. If no **errors** are **detected**, the main processor 100 regards received data as normal data to continue the processing. If a single **error** is **detected** as the **error detection** result, read-out data and a syndrome pattern are latched and the main processor 100 is instructed to retry. In the cycle of retry, latched data is corrected by the syndrome pattern latched by a syndrome latch 280 and is sent to the processor. Thus, **bus** switching is necessary only when a single **error** is **detected**, and the degradation of performance in the normal state, where no errors occur, is suppressed as such as possible.

20/5/20 (Item 3 from file: 347)

DIALOG(R) File 347:JAPIO

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01844229

DECODING DEVICE

PUB. NO.: 61-058329 [JP 61058329 A]
PUBLISHED: March 25, 1986 (19860325)
INVENTOR(s): INOUE TORU
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-180056 [JP 84180056]
FILED: August 29, 1984 (19840829)
INTL CLASS: [4] H03M-013/22
JAPIO CLASS: 42.4 (ELECTRONICS -- Basic Circuits)
JOURNAL: Section: E, Section No. 424, Vol. 10, No. 221, Pg. 132,
August 02, 1986 (19860802)

ABSTRACT

PURPOSE: To reduce the probability of occurrence of error correction to obtain a highly reliable system, by totalizing the number of errors at each stage of decoding in **two directions** performed by means of the 1st and 2nd counters.

CONSTITUTION: Information is inputted from an input terminal 5 and an address is added to the information by means of an address controlling circuit 8, and then, the address-added information is stored in a data RAM 7 through an address **bus** 13 and data **bus** 12. Then a code C(sub 1) is decoded and the decoded results are again stored in the RAM7 and the number

of errors is estimated at every received word. The estimated value is inputted in a counter I.14 and, after the input is made for $n^{(2)}$ times, the error estimated number is summed and accumulated in the counter I.14. Then another code $C^{(2)}$ is decoded and the decoded results are stored in the RAM7. As in the case of the code $C^{(1)}$, the number of errors is estimated at every received word and the estimated value is summed and accumulated in another counter II.15 after the value is inputted for (n) times. A discriminating circuit 16 opens a gate circuit 17 and instructs the circuit 17 to output the decoder's results, when the count values $k^{(1)}$ and $k^{(2)}$ of the circuits 14 and 15 satisfy Formulae I, II. The $d^{(1)}$ and $d^{(2)}$ of the formula are the minimum distances of the codes $C^{(1)}$ and $C^{(2)}$.

?show files;ds

File 621:IAC New Prod.Annou.(R) 1985-1999/Mar 23

(c) 1999 Information Access Co

File 278:Microcomputer Software Guide 1999/Mar

(c) 1999 Reed Elsevier Inc.

File 256:SoftBase:Reviews,Companies&Prods. 85-1999/Feb

(c)1999 Info.Sources Inc

File 647:CMP Computer Fulltext 1988-1999/Mar W2

(c) 1999 CMP

File 674:Computer News Fulltext 1989-1999/Mar W3

(c) 1999 IDG Communications

File 98:General Sci Abs/Full-Text 1984-1999/Feb

(c) 1999 The HW Wilson Co.

File 275:IAC(SM) Computer Database(TM) 1983-1999/Mar 23

(c) 1999 Info Access Co

File 16:IAC PROMT(R) 1972-1999/Mar 23

(c) 1999 Information Access Co.

File 148:IAC Trade & Industry Database 1976-1999/Mar 23

(c) 1999 Info Access Co

Set	Items	Description
S1	29857	BI()DIRECTION? OR BIDIRECTION? OR TWO(2W)DIRECTION? OR "2"- ()DIRECTION? OR MORE()THAN()ONE()DIRECTION? OR DUAL(2W)DIRECT- ION? OR PLURALITY(2W)DIRECTION?
S2	8502	ERROR? ?(3N)(DETECT? AND CORRECT?)
S3	98121	PROGRAMMABLE
S4	3071725	BUS OR EDIT OR BUFFER
S5	2096	(THIRD OR THREE OR TRI? OR TRIPLE?)(2W)BUS
S6	335	S1 AND S2
S7	11	S5 AND S6
S8	216	S4 AND S6
S9	307	S6 AND PY<1998
S10	263	RD (unique items)
S11	55	S1(S)S2
S12	15	S4(S)S11
S13	0	S5(S)S11
S14	48	S11 AND PY<1998
S15	42	RD (unique items)

?t15/3,k/all

>>>KWIC option is not available in file(s): 278

15/3,K/1 (Item 1 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00749090

00749528

VeriBest Integrates Modeling Capabilities for Mechanical Design with VeriBest PCB

PR Newswire

DATELINE: SANTA CLARA, Calif. March 17, 1997 WORD COUNT: 740

...full

analysis capability for both the electronic and mechanical design in one package, enables full **bidirectional** integration of PCB and mechanical design on a single desktop. The end result is a...

...lock-up

positions and detects interference between parts. With ADAMS/MS Motion, users find and **correct** design **errors**, such as colliding parts, before building physical prototypes. These capabilities are most beneficial in the...

15/3,K/2 (Item 2 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00329041

00329041

HARRIS SEMICONDUCTOR ANNOUNCES INDUSTRY'S FIRST RAD HARD CLASS-S ACS/ACTS CMOS LOGIC FAMILY

News Release

DATELINE: Melbourne, FL May 11, 1992 WORD COUNT: 565

...ACTS244

(3-state octal non-inverting buffer/line driver), and ACTS 245(3-state octal **bidirectional** transceiver). All are pin-compatible with LS and ALS TTL-equivalent circuits.

RADIATION PERFORMANCE

Built...

...will make available the ACS/ACTS630, the fastest and most rad hard 16-bit parallel **error detection** and **correction** circuits available for military and aerospace applications. Other devices scheduled for release this summer include...

15/3,K/3 (Item 3 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00298451

00298451

NEW SE 9510 HDDR FORMATTER FROM PENN & GILES FEATURES IEEE- 488/RS449 REMOTE CONTROL AND STATUS INTERFACING

News Release

DATELINE: ROSWELL, GA May 20, 1991 WORD COUNT: 322

...Mbps distributed over up to 32 tape tracks. Incorporated in the unit are an enhanced **error detection** and **correction** system for virtual **error** -free performance, full **bi-directional** operation, and auto-ranging reproduce bit synchronizers.

Modular construction provides the flexibility to adapt for...

15/3,K/4 (Item 4 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00247322

00247322

REMEX INTRODUCES NEW DNC SHOP TERMINAL WITH REMOTE OPERATOR'S KEYBOARD AND DISPLAY

News Release

DATELINE: Fullerton, CA November 29, 1989 WORD COUNT: 419

...the DNC host computer. The MIU is designed to operate with background communications in a **bidirectional** DNC network. It includes a port for the remote operator's pendant.
A card rack...

...flexibility with a variety of optional devices. It can be used for parallel BTR output; **bidirectional** serial input/output to local printers and program loaders; multiport cards with **bi-directional** serial interfaces to other machine tools; parallelpunch input/output; text or graphics display terminals; and...

...chaining for unlimited program length; a 19,200-baud RS-422 data communications port with **error detection** and **correction**; optical isolation from faulty grounds and shorts; multiple file storage; and compact size of only...

15/3,K/5 (Item 5 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00239136

00239136

NATIONAL SEMICONDUCTOR'S FAST TRANSCEIVER GENERATES AND CHECKS PARITY DATA

News Release

DATELINE: SANTA CLARA, CA September 5, 1989 WORD COUNT: 688

...bipolar logic ICs, the 74F899 9-Bit Latchable Transceiver which combines the functions of a **bidirectional** bus transceiver with parity generation and simultaneous check capability. By consolidating the transceiver and parity...

...Typical 74F899 applications are systems that can use byte parity instead of the more complex **error detection** and **correction** (EDAC) schemes. With word sizes up to 64 bits, byte parity requires less routing of...

...equal to two parity generations, i.e., 36 ns (max.). The result is faster data-**error detection** and reduced system cost. Another unique feature of the **bidirectional** 74F899 is the drive capability of its outputs. While the A-bus drive is a...

...This new member of the FAST family of bipolar logic combines the functions of a **bidirectional** bus transceiver with parity generation and simultaneous check capability. This single IC can replace an...

15/3,K/6 (Item 6 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00210832

00210832

MANHATTAN SKYLINE ANNOUNCES THE UM83C001-X WINCHESTER DISK CONTROLLER FROM UNITED MICROELECTRONICS CORP, (UMC)

News Release

DATELINE: Maidenhead, United Kingdom December 12, 1988 WORD COUNT: 302

...separate computer access port enables communications between the host and disk controller. An 8-bit **bi-directional** bus and appropriate control signals comprise this port. UM83C001 address, status & data register, disk read...

...ROM

V.C.O. - Voltage Control Oscillator

All Necessary Receivers and Drivers

Features:

8-bit **bi-directional** interface

IBM XT Winchester controller emulation, IBM PC host interface

Chip set: UM83C001/UM83C003/UM6116...

...available with auto-configuration and splitting

Programmable sector interleave capability

32-bit ECC polynomial for **error detection** and **correction**

Controls up to 2 drivers

Supports drivers of any configuration up to 1024 cylinders and...

15/3,K/7 (Item 7 from file: 621)

DIALOG(R)File 621:IAC New Prod.Annou.(R)

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00206767

00206767

XcelleNet, Inc. Announces Graphics-Based Wide Area Network Product

News Release

DATELINE: ATLANTA, GA October 24, 1988 WORD COUNT: 980

...of a thousand or more remote PCs, with full centralized control over complex events scheduling, **bidirectional** file transfers, and multi-level **error correction** - all done 'invisibly' to remote PCs. And the result of this friendly, controlled support is...

...data compression, full computer control of all sessions, "checkpoint" restarting of interrupted sessions and reliable **error detection** and **correction** all work to ensure maximum throughput. These features have enabled customers to report reductions in...

15/3,K/8 (Item 8 from file: 621)

DIALOG(R)File 621:IAC New Prod.Annou.(R)

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00197169

00197169

NEW REAL-TIME COLOR GRAPHICS SOFTWARE INCREASES MOBILE ROBOT PRODUCTIVITY

News Release

DATELINE: Roanoke, VA August 10, 1988 WORD COUNT: 628

...feet

using dead reckoning alone.

At transaction points the vehicles perform a docking maneuver using **bidirectional** optical communication with a fixed docking beacon. This docking maneuver allows a vehicle to **correct** its accumulated position

error and to align precisely to the pick-up structure.
The vehicles communicate with a host...

15/3,K/9 (Item 9 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00178529

00178529

**SHARENET CONNECTIVITY SOLUTION PROVIDES PRODUCTS AND TECHNOLOGY LICENSING
TO VARS AND OEMS**

News Release

DATELINE: Santa Barbara, CA October 2, 1987 WORD COUNT: 550

...and Hayes-Compatible interfaces, and includes an electronic mail feature. The ShareNet 5110 is a **bi -directional** Parallel port module that can be installed at either the computer or the peripheral end...

...IBM PS/2 and the Data Migration Facility. The ShareNet 5120 has both serial and **bi -directional** parallel ports. The ShareNet 5180 is an IBM-halfcard with dual-ported RAM for OEMs...

...or token-passing techniques. Serial/parallel and baud rate conversion, as well as CRC-based **error detection** and **correction**, are automatic and transparent to the user. The system is masterless, and failure of any...

...calendar.

Pricing for the dual-port model is \$189, the serial model is \$169, the **bi -directional** parallel model is \$149, and the IBM halfcard is \$99. SwitchBoard utility software is \$79...

15/3,K/10 (Item 10 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00164895

00164895

COMPU-MECH INTRODUCES NEW LOW COST "WIRELESS" COMMUNICATION PRODUCTS

DATELINE: Toledo, OH July 30, 1987 WORD COUNT: 518

...over the existing AC power wiring in any building.

The CD8000 Series features:

High speed **bi -directional** serial communications up to 9600 baud over the existing AC power wiring in a building.

High power, noise tolerant powerline carrier current circuitry.

CRC-16 **error detection** and **error correction** algorithms assure data integrity.

Models available with various interface combinations including: RS-232 serial port...

15/3,K/11 (Item 11 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00150711

00150711

IDT offers faster, cooler drop-in replacements for Am2903/203/705/707

DATELINE: Santa Clara, CA March 24, 1987 WORD COUNT: 919

...directional three-port architecture. Easily expandable in 4-bit

increments, the 39C03's ports are **bi -directional** .
IDT Introduces Faster, Cooler Drop-In Replacements for Am2903/
203/705/707
Page 3...

...Drop-in Replacements for Am
2903/203/705/707
Page 5 of 5

register files, **error detector -correctors** and support circuits),
digital signal processing products (high-speed multipliers,
multiplier-accumulators and FIFOs), high...

15/3,K/12 (Item 12 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00139631

00139631

**INTEGRATED DEVICE TECHNOLOGY INTRODUCES THE INDUSTRY'S FASTEST LOGIC
FAMILY, ANNOUNCES SPEED UPGRADE TO EXISTING LOGIC PRODUCTS**

DATELINE: SANTA CLARA, CA October 1, 1986 WORD COUNT: 796

...dual decoders,
synchronous binary counters, carry-lookahead generators, up/down
binary counters, octal buffers, octal **bidirectional** transceivers,
octal D flip-flops, octal universal shift registers, octal
transparent latches, 8-bit comparators...

...MICROSLICE (TM) bit-slice microprocessor family
(4-bit and 16-bit microprocessors, sequencers, register files, **error
detector -correctors** and support circuits), digital signal processing
products (high-speed static RAMs (16K to 64K in...

15/3,K/13 (Item 13 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
(c) 1999 Information Access Co. All rts. reserv.

00129439

00129439

PARADYNE INTRODUCES NEW 19200 BPS MODEM

DATELINE: Largo, FL March 24, 1986 WORD COUNT: 394

...lines using either terrestrial or satellite
communication links. An advanced line impairment monitoring
algorithm, called **bidirectional** adaptive rate control, allows the
modem to operate with changing line conditions at the highest...

...of the
entire range of modem functions such as automatic adaptive
equalization, filtering, modulation/demodulation, **error correction**
and signal conditioning to provide data integrity over a wide range
of operating environments.
The...

15/3,K/14 (Item 14 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
(c) 1999 Information Access Co. All rts. reserv.

00119424

00119424

NEW INSTRUMENTATION TAPE RECORDER/REPRODUCER FROM FAIRCHILD WESTON

DATELINE: Sarasota, FL December 27, 1985 WORD COUNT: 287

...system.
· IRIG head configurations up to 28 tracks.
· Up to 14 inch reel size.
· Eight **bi -directional** tape speeds (120 thru 15/16 ips).
· Built-in test equipment for calibration of both...

...340 watts for full 28 channel system.
· Serial high density digital record and reproduce or **error detection** and **correction** system for parallel high density digital operation at low error rates.
· 28 Volts DC, 117...

15/3,K/15 (Item 15 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
(c) 1999 Information Access Co. All rts. reserv.

00115865

00115865

VM PERSONAL COMPUTING RELEASES, SHIPS RELAY GOLD COMMUNICATIONS SOFTWARE
New Software Package for Microcomputers Features Multi-Tasking, Unique
Script Language

DATELINE: DANBURY, CT September 11, 1985 WORD COUNT: 589

...to and from IBM mainframes using VM
Personal Computing's mainframe package called RELAY/3270. **Error detection** and **correction** are maintained in both directions.
The product increases the productivity of users at all levels...

...supports the public domain protocols KERMIT and XMODEM in addition to its own high performance **bidirectional** protocol. Among the supported modems are the AT&T 2224B, Hayes (including the 2400), Penril...

15/3,K/16 (Item 16 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
(c) 1999 Information Access Co. All rts. reserv.

00114607

00114607

ALLEN-BRADLEY INTRODUCES VISTA AREA MANAGEMENT SYSTEM;
COMPUTER/COMMUNICATIONS CONTROL SCHEME IMPLEMENTS MAP STANDARD

DATELINE: Cleveland, OH August 5, 1985 WORD COUNT: 1011

...Vista 2000 Industrial Computer has up to three megabytes of dynamic random access memory with **error detection** and **correction**. It supports a software operating environment of 16 megabytes of virtual memory for Base Control...

...and provides on-line performance management of the network. The Head-End Remodulator provides for **bidirectional** broadband communication per IEEE 802.4 and GM's MAP specification.
Components of the Vista...

15/3,K/17 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 1999 CMP. All rts. reserv.

00612578 CMP ACCESSION NUMBER: EBN19881017S1474
Saratoga Focuses On RISC - Moves To Larger Fab, Will Upgrade 4-In. Lines
(620)
Teri Sprackland

ELECTRONIC BUYERS' NEWS, 1988 , n 620, 10
PUBLICATION DATE: 881017
JOURNAL CODE: EBN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: 620PG10
WORD COUNT: 911

, 1988

... The proprietary product line will be introduced within six months, he said, and will include **bidirectional** FIFOs, multiport RAMs, **error - detection correction** circuits and four varieties of self-timed RAMs.

Lau sees the company branching out down...

15/3,K/18 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 1999 CMP. All rts. reserv.

00611648 CMP ACCESSION NUMBER: EBN19881212S0543
Add-In Boards (628)
ELECTRONIC BUYERS' NEWS, 1988 , n 628, 44
PUBLICATION DATE: 881212
JOURNAL CODE: EBN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: 628PG44
WORD COUNT: 341

, 1988

... operates in 6-, 8-, 10- or 12-MHz systems; 16-bit data bus, 8-bit **bidirectional** bus for control and status transfers; supports 1:1 interleave; multiple sector read/write commands...

...and error recovery algorithms; read/ write, diagnostic and verify commands; 32- bit ECC for Winchester **error detection and correction** ; drive interface conforms to ST506/ST412 specs.

Price: \$202.50 SRP

Delivery: Off the shelf

15/3,K/19 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 1999 CMP. All rts. reserv.

00534363 CMP ACCESSION NUMBER: EBN19930315S4651
LAST RUNS
ELECTRONIC BUYERS' NEWS, 1993 , n 845, 26
PUBLICATION DATE: 930315
JOURNAL CODE: EBN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: PRODUCTS
WORD COUNT: 734

, 1993

... counter in LCC; SNJ54HC192FK synchronous 4-bit up/down counter in LCC; SNJ54HC194FK 4-bit **bidirectional** universal shift register in LCC; SNJ54LS13W dual 4-input positive NAND Schmitt trigger in flatpack...

...subtractor; SNJ54LS490 dual 4-bit decade counter; SNJ54LS626 voltage controlled oscillator; SNJ54LS630 16-bit parallel **error detection and correction** circuit; SNJ54LS641 octal bus transceiver; SNJ54LS681 4-bit parallel binary accumulator; SNJ54LS693 synchronous counter, registered...

...function generator; SN54LS385 quad serial adder/subtractor; SN54LS626 voltage controlled oscillator; SN54LS630 16-bit parallel **error detection and correction** circuit; SN54LS681 4-bit parallel binary accumulator; SN54LS693 synchronous counter, registered, multiplexed, 3-state outputs...

...5962-86834012A (54HC160) synchronous 4-bit decade counter in LCC;
5962-86826012A (54HC194) 4- bit **bidirectional** universal shift register in
LCC; 5962-8688101RA (54LS382A) arithmetic logic unit/function generator in
DIP...

15/3,K/20 (Item 1 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
(c) 1999 Info Access Co. All rts. reserv.

01948502 SUPPLIER NUMBER: 18373685 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Amazing free stuff. (1,001 best Internet downloads) (includes related
article on Best of the Internet awards) (Directory)**
Noble, Liesl La Grange
PC/Computing, v9, n7, p100(19)
July, 1996
DOCUMENT TYPE: Directory ISSN: 0899-1847 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 17331 LINE COUNT: 01448

... speed file-exchange package to share files with other PCs.
HS/Link: A high-speed, **error -correcting , bidirectional**
file-transfer program that works with your communications software.
MailAway: Use MailAway to transfer files...

19960700

15/3,K/21 (Item 2 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
(c) 1999 Info Access Co. All rts. reserv.

01692943 SUPPLIER NUMBER: 16057410 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Corporate business servers: an alternative to mainframes for business
computing. (HP's 9000 Model T500 file server) (includes related article
on package designing) (Technical)**
Alexander, Thomas B.; Robertson, Kenneth G.; Lindsay, Dean T.; Rogers,
Donald L.; Obermeyer, John R.; Keller, John R.; Oka, Keith Y.; Jones,
Marlin M., II
Hewlett-Packard Journal, v45, n3, p8(23)
June, 1994
DOCUMENT TYPE: Technical ISSN: 0018-1153 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 16095 LINE COUNT: 01283

... illustrated in the memory board block diagram, Fig. 15. 256M-byte
capacity with single-bit **error correction** requires 576 4M-bit DRAMs,
each of which is organized as 1M by 4 bits. 64-byte data transfers and
minimized latency require a 576-bit **bidirectional** data bus for each
bank's DRAMs. The effort to minimize latency and the restriction...

19940600

15/3,K/22 (Item 3 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
(c) 1999 Info Access Co. All rts. reserv.

01666073 SUPPLIER NUMBER: 15050818 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**FAST today, V.fast tomorrow. (Microcom DeskPorte FAST V.fast class modem)
(Hardware Review) (Evaluation)**
Fowler, Dennis
Computer Shopper, v14, n3, p360(1)
March, 1994
DOCUMENT TYPE: Evaluation ISSN: 0886-0556 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 948 LINE COUNT: 00074

...ABSTRACT: The DeskPorte has a useful liquid crystal status display and meets standards for V.42 **error correction** and V.42bis data compression.

19940300

15/3,K/23 (Item 4 from file: 275)

DIALOG(R) File 275:IAC(SM) Computer Database(TM)
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01627563 SUPPLIER NUMBER: 14622789 (USE FORMAT 7 OR 9 FOR FULL TEXT)
You make the call: communications and remote-control software. (includes related articles on shopping tips, file transfer and protocols)
Kawamoto, Wayne
Computer Shopper, v13, n12, p574(9)
Dec, 1993
ISSN: 0886-0556 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4752 LINE COUNT: 00375

... windows" for bidirectional transfers, Kermit can handle 7- or 8-bit data and has an **error -correction** scheme similar to Xmodem's. Kermit tends to be rather slow, but Miss Piggy could...

19931200

15/3,K/24 (Item 5 from file: 275)

DIALOG(R) File 275:IAC(SM) Computer Database(TM)
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01579962 SUPPLIER NUMBER: 13061073 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Things that make you go "huh?": file transfer protocols. (includes related articles on other protocols and on Xmodem's checksum versus cyclical redundancy checking)
Nilsson, B.A.
Computer Shopper, v13, n1, p812(3)
Jan, 1993
ISSN: 0886-0556 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2918 LINE COUNT: 00224

... time. Developed by Communications Research Group.
HS/LINK: Allows bidirectional, multiple-file transfers with an **error -correcting**, streaming technique. It's a shareware program written by Sam Smith (who wrote ProDoor, now...

19930100

15/3,K/25 (Item 6 from file: 275)

DIALOG(R) File 275:IAC(SM) Computer Database(TM)
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01550864 SUPPLIER NUMBER: 13073891 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Pen alignment in a two-pen, large-format, inkjet drafting plotter. (HP's DesignJet drafting plotter) (Technical)
Haselby, Robert D.
Hewlett-Packard Journal, v43, n6, p24(4)
Dec, 1992
DOCUMENT TYPE: Technical ISSN: 0018-1153 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2555 LINE COUNT: 00196

... are variations in inkjet drop velocity. The uncertainty of drop velocity makes it difficult to **correct** for print quality **errors** when printing in a **bidirectional** mode with either single-cartridge or multiple-cartridge printers. Since the drop must travel a...

...repeatable enough so that unidirectional printing results in acceptable

print quality with single-pen printers. **Bidirectional** printing of text is acceptable if the row of text is printed completely in one...

19921200

15/3,K/26 (Item 7 from file: 275)

DIALOG(R)File 275:IAC(SM) Computer Database(TM)
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01550862 SUPPLIER NUMBER: 13073377 (USE FORMAT 7 OR 9 FOR FULL TEXT)
A large-format thermal inkjet drafting plotter. (HP's DesignJet plotter)
(includes related article on user attitudes) (Technical)
Boeller, Robert A.; Stodder, Samuel A.; Meyer, John F.; Escobedo, Victor T.
Hewlett-Packard Journal, v43, n6, p6(10)
Dec, 1992
DOCUMENT TYPE: Technical ISSN: 0018-1153 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 7167 LINE COUNT: 00550

... requires two DeskJet pens to act as one larger pen but also needs to print **bidirectionally** to achieve the throughput goals. Much attention had to be given to the alignment of...

...goal. A scheme was implemented by which pen alignment error in the scan direction and **bidirectional** error (carriage deadband) are measured with an optical sensor. These **errors** are then **corrected** by varying the timing of ink-drop flung.

The difficulty arose when we tried to...

19921200

15/3,K/27 (Item 8 from file: 275)

DIALOG(R)File 275:IAC(SM) Computer Database(TM)
(c) 1999 Info Access Co. All rts. reserv.

01321387 SUPPLIER NUMBER: 07993392 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Build a direction-sensing bidirectional repeater; extend an EIA-485 control bus with an intelligent repeater.
Murdock, Gary; Goldie, John
Electronic Design, v37, n10, p105(5)
May 11, 1989
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2510 LINE COUNT: 00184

ABSTRACT: Direction-sensing **bidirectional** signal repeaters can extend an EIA-485 control bus through the amplification of signals, increase...

...necessary for distances in excess of one cable segment. A circuit for a direction-sensing **bidirectional** repeater can be developed that consists of two standard-pinout EIA-485 transceivers. The repeater has six functional blocks: **bidirectional** repeater, data line state sensor; circuitry for determining enable signals; pulse generator for masking, clocking and **error** signals; filter and **detector** of valid line state changes; and enable signal generator. Details of the repeater design are...

19890511

15/3,K/28 (Item 9 from file: 275)

DIALOG(R)File 275:IAC(SM) Computer Database(TM)
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01305561 SUPPLIER NUMBER: 07427712 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Bidirectional buffering speeds RISC-to-SCSI communication. (includes a related article on a bidirectional FIFO buffer) (two-way buffering

matches 32-bit reduced instruction set computing bus to 8-bit peripheral channel)

Eidson, Steven; Lengoc, Danh; Lin, Julie

Electronic Design, v37, n15, p67(6)

July 13, 1989

ISSN: 0013-4872

LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT; ABSTRACT

WORD COUNT: 2064

LINE COUNT: 00161

...ABSTRACT: speed throughput but the processor must be ready to relinquish the bus on short notice. **Error detection and correction** should also be incorporated into peripheral channels. A **bidirectional** first-in first-out (FIFO) buffer offers the best solution to the problem of linking processors with unequal transmission rates. A design using two **bidirectional** FIFOs in parallel to produce a 36-bit to 9-bit RISC-SCSI interface is...

... least-significant byte order or vice versa.

NO ERRORS ALLOWED

Many peripheral devices have incorporated **error -correction -coding** (ECC) techniques. These coding techniques offer adequate protection against errors for the peripheral-controller...

...Because the data is being transmitted between the RISC processor and the peripheral through the **bidirectional** FIFO buffer, the buffer should generate parity and **detect** parity errors .

The RISC-based system memory-interface block consists of a write buffer, a read buffer...

19890713

15/3,K/29 (Item 10 from file: 275)

DIALOG(R) File 275:IAC(SM) Computer Database(TM)

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01250835 SUPPLIER NUMBER: 06790471 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Pc-board testing arises from CAE simulation vectors. (printed circuit boards) (computer-aided engineering)

Schmeling, Garth

Electronic Design, v36, n13, p123(3)

June 9, 1988

ISSN: 0013-4872

LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT

WORD COUNT: 1345

LINE COUNT: 00107

... any incompatibilities between the HP 3065 board tester and the simulation stimulus and results are **detected** during test generation, **error** or warning messages show the type of error and flag the test vectors affected. These...

...consist of drive signals changing state, receive signals changing state, ambiguous direction being for a **bidirectional** signal during a test cycle, a test-vector cycle taking less than 200 ns or...

19880609

15/3,K/30 (Item 1 from file: 16)

DIALOG(R) File 16:IAC PROMT(R)

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01212805

THE DMX-6000 DISTRIBUTED MEASUREMENT SYSTEM.

MECHANICAL ENGINEERING May, 1985 p. 40-421

Publication Year: 1985

... either in the field or remotely. The master station polls each transmitter and has a **bi -directional** RX-232 port for data communication with a host computer, personal computer or flow computer...

... with microprocessor-based devices, in both the field and the control room, allow for effective **error detection and correction** .

15/3,K/31 (Item 1 from file: 148)
DIALOG(R)File 148:IAC Trade & Industry Database
(c) 1999 Info Access Co. All rts. reserv.

10167376 SUPPLIER NUMBER: 20251572 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The causality effects of the Federal Reserve's monetary policy on U.S. and eurodollar interest rates. (includes appendix)
Mougoue, Mbodja; Wagster, John
Financial Review, v32, n4, p821(24)
Nov, 1997
ISSN: 0732-8516 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5908 LINE COUNT: 00489

... because of increasing financial-market integration.
Fung and Isberg (5) use daily data and an **error correction** model (ECM) to test for causality during the 1981-1988 period. During the 1981-1983 subperiod they find unidirectional causality and during the 1984-1988 subperiod they find **bi-directional** causality. Fung and Isberg's (5) results contradict Swanson's (15,16) findings of **bi-directional** causality during 1981 and reverse uni-directional causality during 1982 and 1983. Fung and Isberg...

19971100

15/3,K/32 (Item 2 from file: 148)
DIALOG(R)File 148:IAC Trade & Industry Database
(c) 1999 Info Access Co. All rts. reserv.

10023956 SUPPLIER NUMBER: 20310230 (USE FORMAT 7 OR 9 FOR FULL TEXT)
An empirical investigation of the causal relationship between openness and economic growth in China.
Lie, Xiaming; Song, Haiyan; Romilly, Peter
Applied Economics, v29, n12, p1679(8)
Dec, 1997
ISSN: 0003-6846 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 5561 LINE COUNT: 00454

... and those in transition. Section II of this paper provides a theoretical discussion of the **bi-directional** openness-growth debate. Section III discusses the methodological approach used in the paper, and Section...

...of the data are analysed and cointegration tests are carried out to determine whether an **error correction** model is needed. Then the models of Granger (1969), Sims (1972), Geweke et al. (1983...

19971200

15/3,K/33 (Item 3 from file: 148)
DIALOG(R)File 148:IAC Trade & Industry Database
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09991873 SUPPLIER NUMBER: 20189114 (USE FORMAT 7 OR 9 FOR FULL TEXT)
In picking ECCs, the key is bit-error location - not rate. (error-correction-codes)
Waschura, Tom
EDN, v42, n23, p163(4)
Nov 6, 1997
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 3206 LINE COUNT: 00263

... bits. The choices of how to handle errors range from doing nothing to using elaborate **error -detection** and **-correction** methods. Selecting among the choices depends on the information's accuracy, speed, and latency requirements and whether simultaneous **bidirectional** communication exists between the sender and the receiver.

An application's intended use of data...

...Bidirectional communication allows for creating systems that achieve low BERs by using powerful and simple **error detection** that asks the transmitter to resend incorrectly received data. This concept is the basis of...

...in magnetic recording systems that verify the data they write while they are writing it. **Errors detected** during writing can trigger the replacement of erroneous data blocks in anticipation of trouble during...

19971106

15/3,K/34 (Item 4 from file: 148)

DIALOG(R)File 148:IAC Trade & Industry Database

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09833117 SUPPLIER NUMBER: 18926682 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Temporal causality and the dynamics of different categories of crime and their socioeconomic determinants: evidence from Australia.

Masih, Abul M.M.; Masih, Rumi

Applied Economics, v28, n9, p1093(12)

Sep, 1996

ISSN: 0003-6846 LANGUAGE: English RECORD TYPE: Fulltext

WORD COUNT: 7976 LINE COUNT: 00899

... not in the structural sense), must exist in at least one direction either unidirectional or **bi -directional** (Granger, 1986, 1988). Evidence of cointegration among variables also rules out the possibility of the...

...direction of causality between variables. This direction of the Granger (or temporal) causality can be **detected** through the vector **error correction** model derived from the long-run cointegrating vectors.

Vector error correction modelling (VECM) and causality...

19960900

15/3,K/35 (Item 5 from file: 148)

DIALOG(R)File 148:IAC Trade & Industry Database

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09414694 SUPPLIER NUMBER: 19291202 (USE FORMAT 7 OR 9 FOR FULL TEXT)

The U.S. dollar in global money markets: a multivariate cointegration analysis.

Lin, Antsong; Swanson, Peggy E.

Quarterly Review of Economics and Finance, v37, n1, p139(12)

Spring, 1997

ISSN: 1062-9769 LANGUAGE: English RECORD TYPE: Fulltext; Abstract

WORD COUNT: 4372 LINE COUNT: 00376

... London to New York than from New York to London as indicated by a significant **error correction** term coefficient in the London to New York equation.

Bidirectional impacts are found between the...

...the domestic to the Hong Kong market) is greater than reverse causality based on the **error correction** term coefficients; however, equally significant **bidirectional** short-term causality is found.

The relationship between the London dollar market and the two...

...market; the only causality indicated from Hong Kong to the London market occurs through the **error correction** term while the London market

impacts Hong Kong also via lagged London rates (but only...

19970300

15/3,K/36 (Item 6 from file: 148)

DIALOG(R)File 148:IAC Trade & Industry Database

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08134731 SUPPLIER NUMBER: 17415961 (USE FORMAT 7 OR 9 FOR FULL TEXT)

The dynamics and competitiveness of European-Asian trade flows. (Euro-Asian Management and Business I - Cross-border Issues) (Section 3: Cross-border Trade Flows and Risk Management)

Parhizgari, Ali M.

Management International Review, v35, nSPEISS, p151(11)

Annual, 1995

ISSN: 0025-181X LANGUAGE: English

RECORD TYPE: Fulltext; Abstract

WORD COUNT: 3198 LINE COUNT: 00283

...ABSTRACT: without resolving the complex battery of economic models (explanations) currently available, the one- or the **bi-directional** relationship(s) that may exist between these two terminal variables. Using an **error correction** model, the dynamics of the above relationship(s) in terms of the lag structure and...

... also included. Considering these measures and based on both the standard Granger case and the **error correction** model, the results indicate considerable degree of **bi-directional** causality (feedback) in the series. The only exception is Japanese import (JM) which does not...

...MM (Table 6, panel A), causality is barely supported by the F-value in the **error correction** model. The ECM also establishes causality from MX to ECU via the ECM term. The...

19950000

15/3,K/37 (Item 7 from file: 148)

DIALOG(R)File 148:IAC Trade & Industry Database

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08121254 SUPPLIER NUMBER: 17380983 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Long-run money demand function in Argentina during 1935-1962: evidence from cointegration and error correction models.

Choudhry, Taufiq

Applied Economics, v27, n8, p661(7)

August, 1995

ISSN: 0003-6846 LANGUAGE: English

RECORD TYPE: Fulltext

WORD COUNT: 4220 LINE COUNT: 00372

... also evidence of a feedback between the rate of inflation and real money stock. The **error correction** term is only significant in the inflation rate equation and this is true in both periods in all four relationships. Significance of the **error correction** in the inflation equation implies that the rate of inflation adjusted to changes in the...

...four money equations, thus providing evidence of real money stock adjusting to the inflation. Thus, **bidirectional** causality between the real M1 or the real M2 and the rate of inflation is...

...and changes were implemented in 1946 resulting in more economic variability. Using cointegration tests and **error correction** modelling, we investigate the relationship between real M1 or real M2, the rate of inflation...

...and real M2) maintained a stationary long-run relationship with the stated variables. Results from **error correction** models provide evidence of **bidirectional** causality between the real money balances and the inflation rate. Real income is purely exogenous...

19950800

15/3,K/38 (Item 8 from file: 148)

DIALOG(R)File 148:IAC Trade & Industry Database
(c) 1999 Info Access Co. All rts. reserv.

07820730 SUPPLIER NUMBER: 15484877 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Cointegration and error correction models: the temporal causality between investment and corporate cash flow.

Mahdavi, Saeid; Sohrabian, Ahmad; Kholdy, Shady

Journal of Post Keynesian Economics, v16, n3, p478(21)

Spring, 1994

ISSN: 0160-3477 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT

WORD COUNT: 7902 LINE COUNT: 00648

... then incorporated the information provided by such a relationship into our causality analysis by specifying **error correction** models. In what follows, we provide a brief formal discussion of the concepts of stationarity...

19940322

15/3,K/39 (Item 9 from file: 148)

DIALOG(R)File 148:IAC Trade & Industry Database
(c) 1999 Info Access Co. All rts. reserv.

07620717 SUPPLIER NUMBER: 16031597 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Fast CNC boosts machine-tool accuracy. (computer numerical control products from GE Fanuc Automation) (Product Announcement)

American Machinist, v138, n12, p14(1)

Dec, 1994

DOCUMENT TYPE: Product Announcement ISSN: 1041-7958 LANGUAGE:
ENGLISH RECORD TYPE: FULLTEXT

WORD COUNT: 445 LINE COUNT: 00037

... special options.

New compensation features help improve machine-tool accuracy. Interpolation pitch-error compensation and **bidirectional** pitch-error compensation **correct** lead-screw inaccuracies. Nonorthogonal axes are not a problem because of interpolated straightness compensation. And...

19941200

15/3,K/40 (Item 10 from file: 148)

DIALOG(R)File 148:IAC Trade & Industry Database
(c) 1999 Info Access Co. All rts. reserv.

07237316 SUPPLIER NUMBER: 15112675 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Cointegration and market integration: an application to the Indonesian rice market.

Alexander, Carol; Wyeth, John

Journal of Development Studies, v30, n2, p303(32)

Jan, 1994

ISSN: 0022-0388 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT

WORD COUNT: 10563 LINE COUNT: 00815

... be bidirectional causality) may be tested using the unrestricted form (6) and (7) of the **error correction** model, as in Alexander |1993

. Rejection of the joint hypothesis:

||Theta

.sub.21

= . . . ||Theta

.sub...

19440100

15/3,K/41 (Item 11 from file: 148)
DIALOG(R) File 148:IAC Trade & Industry Database
(c) 1999 Info Access Co. All rts. reserv.

05583244 SUPPLIER NUMBER: 11688330 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Drive ICs: ASICs or off-the-shelf? Cost, time-to-market pressures rule
choice, say drive makers. (integrated circuits, application-specific
integrated circuits)

Arnold, Bill
EDN, v36, n24A, p1(3)
Nov 28, 1991

ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1641 LINE COUNT: 00130

... to control read and write bits through the buffer memory, and a
controller to translate **bidirectional** data and perform **error**
correction. A second National Semiconductor HPC controls the servo
channel, he adds.

For its 90- and...

19911128

15/3,K/42 (Item 12 from file: 148)
DIALOG(R) File 148:IAC Trade & Industry Database
(c) 1999 Info Access Co. All rts. reserv.

02823812 SUPPLIER NUMBER: 04264158 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Bubbles on the rise. (bubble memory)

Cooper, Paul V.; MacIntosh, Peter M.
Defense Electronics, v18, p139(7)
June, 1986

ISSN: 0278-3479 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 3118 LINE COUNT: 00249

... 2 megabytes, all the dedicated analog circuits and the bubble
memory control, redundancy management, and **error detection** and control
(EDC) logic. The maximum data rate of the memory board via the
bidirectional 8-bit bus is 1.6 megabits per second. The average access
time to a...

19860600

?

```
?show files;ds
File 108:Aerospace Database 1962-1999/Feb
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(c) 1999 Reed Reference Publishing
File 239:Mathsci(R) 1940-1999/Mar
(c) 1999 American Mathematical Society
File 233:Microcomputer Abstracts 1974-1999/Mar
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(c) 1998 Inst for Sci Info
File 62:SPIN(R) 1975-1999/Feb W3
(c) 1999 American Institute of Physics
File 99:Wilson Appl. Sci & Tech Abs 1983-1999/Feb
(c) 1999 The HW Wilson Co.
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Set	Items	Description
S1	42282	BI()DIRECTION? OR BIDIRECTION? OR TWO(2W)DIRECTION? OR "2"- ()DIRECTION? OR MORE()THAN()ONE()DIRECTION? OR DUAL(2W)DIRECT- ION? OR PLURALITY(2W)DIRECTION?
S2	14443	ERROR? ?(3N)(DETECT? AND.CORRECT?)
S3	80828	PROGRAMMABLE
S4	203281	BUS OR EDIT OR BUFFER
S5	530	(THIRD OR THREE OR TRI? OR TRIPLE?)(2W)BUS
S6	52	S1 AND S2
S7	0	S5 AND S6
S8	9	S4 AND S6
S9	52	S6 AND PY<1998
S10	36	RD (unique items)

?t10/7/all

10/7/1 (Item 1 from file: 108)
DIALOG(R)File 108:Aerospace Database
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01740765 A88-36474

ARQ scheme reinforced with past acknowledgement signals (Automatic Repeat-reQuest)

NAKAMURA, MAKOTO; TAKADA, YASUSHI (Toshiba Corp., Toshiba Research and Development Center, Kawasaki, Japan)

IN: GLOBECOM '87 - Global Telecommunications Conference, Tokyo, Japan, Nov. 15-18, 1987, Conference Record. Volume 3 (A88-36401 14-32). New York, Institute of Electrical and Electronics Engineers, Inc., 1987, p. 2100-2104.

1987 8 REFS.

LANGUAGE: English

COUNTRY OF ORIGIN: Japan COUNTRY OF PUBLICATION: United States

DOCUMENT TYPE: CONFERENCE PAPER

DOCUMENTS AVAILABLE FROM AIAA Technical Library

JOURNAL ANNOUNCEMENT: IAA8814

An ARQ (automatic-repeat-request) scheme that can reduce the influence of backward channel errors for **bidirectional** data transmission systems is proposed. The main feature of the scheme is that both present and past acknowledgement signals are utilized to decide whether the data signals should be retransmitted or not. Throughput performance is analyzed in both go-back-N and selective-repeat ARQ. A small number of returned past acknowledgement signals are required to improve the throughput efficiency. For an ideal selective-repeat ARQ with an infinite buffer, increasing the number of returned past acknowledgement signals makes the throughput efficiency asymptotically close to the upper bound (I.E.)

SOURCE OF ABSTRACT/SUBFILE: AIAA

10/7/2 (Item 2 from file: 108)
DIALOG(R)File 108:Aerospace Database
(c) 1999 AIAA. All rts. reserv.

01715121 A88-10829

Satellite measurements of the earth radiation budget: Sampling and retrieval of short wave exitances - A sampling study

STUHLMANN, R.; RASCHKE, E. (Koeln, Universitaet, Cologne, Federal Republic of Germany)

Beitraege zur Physik der Atmosphaere (ISSN 0005-8173), vol. 60, Aug. 1987, p. 393-410.

Aug. 1987 39 REFS.

CONTRACT NO.: BMFT-01-05-080-5

LANGUAGE: English

COUNTRY OF ORIGIN: Germany COUNTRY OF PUBLICATION: Germany

DOCUMENT TYPE: JOURNAL ARTICLE

DOCUMENTS AVAILABLE FROM AIAA Technical Library

JOURNAL ANNOUNCEMENT: IAA8801

The effects of uncertainties in the filter and **bidirectional** correction on the accuracy of single and regionally averaged values of the upward radiation flux inverted, using the process of Smith et al. (1986), from satellite radiance data are investigated. The filter and **bidirectional** reflectance functions for the earth radiation budget experiment and Meteosat sensors were calculated; it is observed that relative uncertainties in single values due to the filter correction range between 1-2 percent for the broad-band instrument and between 10-25 percent for the Meteosat radiometer, and for **bidirectional** reflectance corrections the uncertainties range from 5 to 25 percent for single values in both cases. The propagation of errors through the spatial integration is examined using an earth radiation model. It is detected that for the narrow-band instrument the error of the filter function is reduced to about 2-7 W/sq m and for the **bidirectional correction** the **error** is between 8 and 23 W/sq m. (I.F.)

SOURCE OF ABSTRACT/SUBFILE: AIAA

10/7/3 (Item 3 from file: 108)
DIALOG(R)File 108:Aerospace Database
(c) 1999 AIAA. All rts. reserv.

01405207 N82-10323

CCD/MOS sampled analog IMS adaptive signal processor

Ph.D. Thesis

MAZUMDAR, S.

Polytechnic Inst. of New York, Brooklyn.

CORPORATE CODE: PZ176914

1981 138P.

LANGUAGE: English

COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: United States

DOCUMENT TYPE: THESIS

DOCUMENTS AVAILABLE FROM AIAA Technical Library

OTHER AVAILABILITY: Univ. Microfilms Order No. 8118886

JOURNAL ANNOUNCEMENT: STAR8201

An all analog adaptive signal processor applying the least mean square error algorithm is described. This processor is primarily a transversal filter. A simple MOSFET multiplier is developed in conjunction with a **bidirectional** charge integrator, providing advantages in speed, cost, power consumption, and weight over digital and hybrid adaptive processors. A feasibility study of different analog multipliers for use in an analog adaptive processor, an analysis of the errors introduced by the various devices are presented. The effects of these errors on the processor performance are considered. The processor compensates for the errors introduced by most of the components except for any offset error introduced by the tap weight charge integrator and by the comparator that detects the difference between the reference signal and the processor output. Applications for the processor are outlined (Dissert. Abstr.)

SOURCE OF ABSTRACT/SUBFILE: Dissert. Abstr.

10/7/4 (Item 4 from file: 108)
DIALOG(R)File 108:Aerospace Database
(c) 1999 AIAA. All rts. reserv.

01303245 N81-10714

Mutation analysis of program test data

Ph.D. Thesis

BUDD, T. A.

Yale Univ., New Haven, CT.

CORPORATE CODE: YE661058

1980 155P.

LANGUAGE: English

COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: United States

DOCUMENT TYPE: THESIS

DOCUMENTS AVAILABLE FROM AIAA Technical Library

OTHER AVAILABILITY: Univ. Microfilms Order No. 8025191

JOURNAL ANNOUNCEMENT: STAR8101

Mutation analysis asserts that those test cases are important which differentiate, in the sense of being correctly processed by one and incorrectly processed by the other, the original program from programs very similar in structure and meaning. These alternative programs are called mutants of the original. The power of this method is further increased by two observations: the coupling effect which asserts that complex errors can often be detected by the analysis of a small set of simple alternatives; and the competent programmer hypothesis, which asserts that most programs are, when they reach the stage of development considered here, a close approximation to being correct. The mutation analysis method is first described in very general terms. Two very different directions are pursued: The first is to give formal meanings to the terms mutants, errors, coupling effect, and competent programmer and prove in a restricted programming domain a theorem concerning the coupling of simple and complex errors. Several results of this nature are proved for decision tables and for a set of linear recursive LISP programs. The second direction is to

study a realistic programming language and to ask whether in a statistical sense the coupling effect occurs. A system to implement mutation analysis for FORTRAN programs is described and compared to other testing methods. Several further studies using this system are described, including analyses of the system's **error detection** capabilities, the machine and human resources it requires, and difficulties involved in using it. The last includes the problem of deciding whether a program and its mutant are computationally equivalent. A summary and a discussion of five possible areas for future research are included (Dissert. Abstr.)

SOURCE OF ABSTRACT/SUBFILE: Dissert. Abstr.

10/7/5 (Item 5 from file: 108)

DIALOG(R)File 108:Aerospace Database

(c) 1999 AIAA. All rts. reserv.

00569478 A73-15426

Coded communication link for an advanced manned spacecraft. (Digital link for **bidirectional** communication between manned spacecraft and ground terminal by synchronous communication relay satellite, noting coding parameters effects on error rate)

GOULD, L. M.; CURRY, S. J. (Hughes Aircraft Co., El Segundo, Calif.); TEASDALE, W. E. (NASA, Manned Spacecraft Center, Houston, Tex.)

In: NTC '72; National Telecommunications Conference, Houston, Tex., December 4-6, 1972, Record. (A73-15376 04-07) New York, Institute of Electrical and Electronics Engineers, Inc., 1972, p. 28F-1 to 28F-6.

1972

LANGUAGE: English

COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: United States

DOCUMENT TYPE: CONFERENCE PAPER

JOURNAL ANNOUNCEMENT: IAA7304

An analysis, in terms of key design parameters, is presented of a digital link for **bidirectional** communication between an advanced manned spacecraft, such as the space shuttle, and a ground terminal by means of a synchronous communication relay satellite. Performance of both ground to manned spacecraft and return links are compared with and without coding. A breadboard terminal for simulating the two-way link is described. Results of error rate tests are discussed (M.V.E.)

SOURCE OF ABSTRACT/SUBFILE: AIAA

10/7/6 (Item 1 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

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03740001 E.I. No: EIP93040768728

Title: Proceedings of the 1993 IEEE International Symposium on Information Theory

Author: Anon (Ed.)

Conference Title: Proceedings of the 1993 IEEE International Symposium on Information Theory

Conference Location: San Antonio, TX, USA Conference Date: 19930117-19930122

Sponsor: IEEE

E.I. Conference No.: 18102

Source: Proceedings of the 1993 IEEE International Symposium on Information Theory Proc 93 IEEE Int Symp Inf Theor 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. 443p

Publication Year: 1993

ISBN: 0-7803-0878-6

Language: English

Document Type: CP; (Conference Proceedings) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 9312W4

Abstract: The Symposium materials contain 443 papers. The topics covered include code optimization; binary sequences generation; signal detection; data fusion; reduced-state sequence detectors; Viterbi algorithms; soft decision decoding; **error correcting** codes; Gaussian multiple access

channels; equalization techniques; redundancy of universal codes; entropy; rate-distortion computation; joint signal detection/estimation; transient signals detection; decentralized encoding; parameter estimation; channels with memory; fault-tolerant distributed decoding; Rayleigh fading; likelihood methods in imaging; **bidirectional** decoding; data compression; role of information theory in emission tomography; vector quantization; communication networks; synchronization games; digital signature schemes; jump-diffusion processes; Huffman algebras; routing algorithms; finite-state models; switching networks; binary trees; trellis codes; wavelet approximation of signals; protocol sequences for multiaccess collision channel; systolic algorithms; Occam-based learner; neural network training; sampling strategies; theory of information transfer; radar waveform design; perceptron algorithms; neural network pattern classifiers; signal filtering; greedy codes; Costas arrays; and sigma-delta modulation.

10/7/7 (Item 2 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

(c) 1999 Engineering Info. Inc. All rts. reserv.

03699389 E.I. No: EIP93071023730

Title: Multibit correcting data interface for fault-tolerant systems

Author: Redinbo, G. Robert; Napolitano, Leonard M. Jr.; Andaleon, David D.

Corporate Source: Univ of California, Davis, CA, USA

Source: IEEE Transactions on Computers v 42 n 4 Apr 1993. p 433-446

Publication Year: 1993

CODEN: ITCOB4 ISSN: 0018-9340

Language: English

Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 9310W5

Abstract: Failures of complex integrated circuits in modern computer systems can affect several bits simultaneously, easily overwhelming standard commercially available correction or detection subassemblies. A fault-detecting, **bidirectional** data interface between uncoded data from one part, such as a processor, and coded data in the rest of the system is described. This interface is capable of correcting a single multibit symbol **error** or **detecting** the occurrence of two such errors. The device uses a shortened Reed-Solomon code and two practical symbol sizes are considered; nibble (4-bit) errors are protected by a (40, 32) binary equivalent shortened code while byte errors are covered by a (80, 64) binary-sized code. The Reed-Solomon codes have maximum protection levels, even when shortened, and allow simplifying design options. A dual orthogonal basis used for the symbols' representations provides significant hardware savings. The interface unit achieves internal fault detection, sensing any single subassembly failure, by comparing regenerated parity values in a totally self-checking equality checker. The probability of undetected error and memory reliability values are easily calculated since the weight distributions for shortened Reed-Solomon codes are developed. A fault-tolerant ultra-reliable memory module is proposed and its reliabilities evaluated. An example design for a nibble-correcting interface is realized using a single desktop programmable gate array and requires a fault detection overhead in module count of about 15%. (Author abstract) 22 Refs.

10/7/8 (Item 3 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

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03433162 E.I. Monthly No: EIM9205-027748

Title: A symbol correcting, fault-tolerant bus interface chip.

Author: Redinbo, G. Robert; Napolitano, Leonard M. Jr.; Andaleon, David D.

Corporate Source: Sandia Nat Lab, Livermore, CA, USA

Conference Title: 1990 (24th) Asilomar Conference on Signals, Systems and Computers Part 2 (of 2)

Conference Location: Pacific Grove, CA, USA Conference Date: 19901105
Sponsor: IEEE Computer Society; Naval Postgraduate School, Monterey, CA, USA

E.I. Conference No.: 16228

Source: Conference Record. Twenty-fourth Asilomar Conference on Signals, Systems and Computers 90 Asilomar Conf. on Signals, Syst. & Comput. Conference Record - Asilomar Conference on Circuits, Systems & Computers v 2. Publ by Maple Press, Inc, San Jose, CA, USA (IEEE cat n 91CH2988-4). p 902-906

Publication Year: 1991

CODEN: RACSDI ISSN: 0736-5861

Language: English

Document Type: PA; (Conference Paper) Treatment: T; (Theoretical)

Journal Announcement: 9205

Abstract: A fault-tolerant, **bi-directional** data interface between uncoded data from one part, such as a processor, and coded data in the rest of the system is described. This interface is capable of correcting a single multi-bit symbol **error** or **detecting** the occurrence of two such errors. The device uses a shortened Reed-Solomon code and two practical symbol sizes, nibble or byte widths, are considered. The class of Reed-Solomon codes have maximum protection levels, even when shortened, and allow simplifying design options. A dual orthogonal basis used for the symbols' representations provides significant hardware savings. The interface unit achieves fault tolerance, detecting any single subassembly failure, by comparing regenerated parity values in a totally self-checking equality checker. An example design for a nibble-correcting interface is realized using a single desktop programmable gate array and requires a fault tolerance overhead of about 15%. 13 Refs.

10/7/9 (Item 4 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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03386141 E.I. Monthly No: EIM9202-010536

Title: **Low-cost transponder system for data transmission to trains in remote areas.**

Author: Hill, R. John; Palmer, Jerry W.; Barnard, Robert E.

Corporate Source: Sch of Electr Eng, Univ of Bath, UK

Conference Title: 1990 ASME/IEEE Joint Railroad Conference

Conference Location: Chicago, IL, USA Conference Date: 19900417

Sponsor: IEEE Vehicular Technology Soc; ASME; ASCE

E.I. Conference No.: 15856

Source: IEEE Technical Papers Presented at the Joint ASME/IEEE/AAR Railroad Conference (Association of American Railroads). Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2947-0). p 117-126

Publication Year: 1990

CODEN: ITPCDZ

Language: English

Document Type: PA; (Conference Paper) Treatment: A; (Applications)

Journal Announcement: 9202

Abstract: Intermittent transmission of geographical location information or command data to moving trains may be achieved by track-mounted transponders. A need for inexpensive, passive transponders that require no electronics in the track equipment exists in remote areas. A metal-plate transponder system, in which information is encoded in the plate pattern as laid between the running rails, is studied. The design problems are to devise reliable plate detector hardware and to select suitable decoding algorithms, and to achieve protection against erroneous bit detection and incomplete reading of the message bits. The design principles and performance characteristics are stated in detail. The system demonstrates the feasibility of **bidirectional** decoding with **dual direction** and orientation capability, low-speed detection, including stopping over the transponder, high speed detection (with timing validation), and error control, including single-**error correction**. 11 Refs.

10/7/10 (Item 5 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)
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03320693 E.I. Monthly No: EIM9110-052137

Title: Storing pattern pairs in a bicameral neural network.

Author: Kak, Subhash C.; Das, Sanjoy

Corporate Source: Dept of Electr & Comput Eng, Louisiana State Univ,
Baton Rouge, LA, USA

Conference Title: IEEE Proceedings of Southeastcon '90 - Technologies
Today and Tomorrow

Conference Location: New Orleans, LA, USA Conference Date: 19900401

Sponsor: IEEE Region 3; South Central Bell; Northern Telecom Inc; AT&T
Network Systems; Louisiana Power & Light Co; et al

E.I. Conference No.: 14990

Source: Conference Proceedings - IEEE SOUTHEASTCON v 2. Publ by IEEE,
IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2883-7). p 489-494

Publication Year: 1990

CODEN: CPISDM ISSN: 0734-7502

Language: English

Document Type: PA; (Conference Paper) Treatment: A; (Applications); T;
(Theoretical); X; (Experimental)

Journal Announcement: 9110

Abstract: A model of a bicameral neural network proposed by S. C. Kak and
M. C. Stinson (Electronics Letters, vol. 25, pp. 203-205, 1989) is examined
for its performance as a heteroassociative memory and for its ability to
store pairs of patterns. The model is **bidirectional**, as any pattern of
each pair can be used as a probe to retrieve the other pattern associated
with it. Issues relating to the **error -correcting** capability of this
model have been investigated experimentally. A method of **detecting** the
errors using a technique called indexing is discussed. A method of
upgrading the model to store patterns sets of more than two patterns each,
such that any one of the patterns in the set could be used as a probe to
retrieve all other patterns associated with it, is discussed. The results
of comparing the **error -correcting** ability of the bicameral model to
that of **bidirectional** associative memory show that the bicameral model
compares favorably. 5 Refs.

10/7/11 (Item 6 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)
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03103471 E.I. Monthly No: EI9108089787

Title: Multiple unidirectional byte error- correcting codes.

Author: Saitoh, Yuichi; Imai, Hideki

Corporate Source: Div of Electr & Comput Eng, Yokohama Nat Univ,
Hodogaya-ku, Yokohama, Japan

Source: IEEE Transactions on Information Theory v 37 n 3 pt II May 1991 p
903-908

Publication Year: 1991

CODEN: IETTAW ISSN: 0018-9448

Language: English

Document Type: JA; (Journal Article) Treatment: A; (Applications); T;
(Theoretical)

Journal Announcement: 9108

Abstract: Codes **correcting /detecting** unidirectional byte **errors** are
investigated. It is shown that such codes have the capability of correcting
combinations of **bidirectional** and unidirectional byte errors and code
constructions. These are derived from the combination of two codes. One is
a code for encoding the Hamming weights of data bytes and is used to
estimate error locations. The other is a byte-**error -correcting** code for
error evaluation. Moreover, the authors describe a decoding procedure for
the codes, correcting combinations of **bidirectional** and unidirectional
byte errors. The constructions provide many efficient codes of short
length. For example, when a byte consists of 32 bits, a systematic code can
be constructed with 61 information bytes and 3 check bytes that has the
capability of correcting a single **bidirectional** byte error for double
unidirectional byte errors, whereas the best known double-byte-**error** -

correcting code requires 4 check bytes. 20 Refs.

10/7/12 (Item 7 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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03051814 E.I. Monthly No: EIM9104-015731

Title: An error corrector / detector implemented in a desktop programmable gate array.

Author: Napolitano, Leonard M. , Jr.; Andaleon, David D.; Shreeve, William O.; Redinbo, G. Robert

Corporate Source: Sandia Nat Lab, Livermore, CA, USA

Conference Title: 1990 IEEE International Symposium on Circuits and Systems Part 1 (of 4)

Conference Location: New Orleans, LA, USA Conference Date: 19900501

Sponsor: IEEE Circuits and Systems Soc

E.I. Conference No.: 14054

Source: Proceedings - IEEE International Symposium on Circuits and Systems v 1. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2868-8). p 21-24

Publication Year: 1990

CODEN: PICSDI ISSN: 0271-4310

Language: English

Document Type: PA; (Conference Paper) Treatment: X; (Experimental); T; (Theoretical)

Journal Announcement: 9104

Abstract: A complete design is presented for an **error detection** or **correction** (EDOC) device based on 32-b data lines to be incorporated as a **bidirectional** buffer between a processor and the rest of the system. The device is internally fault-tolerant itself. The design includes scan-path capability so that the internal state of the chip can be determined during system testing and debugging. This design can correct single-nibble (4-b) **errors** or **detect** double-nibble (8-b) errors, but not both simultaneously. It is implemented in the desktop programmable gate array technology. 6 Refs.

10/7/13 (Item 8 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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01882556 E.I. Monthly No: EIM8508-042962

Title: 4-CHANNEL SUPER-HETERODYNE BIDIRECTIONAL NETWORK ANALYSER WITH VECTOR-NULL DETECTION.

Author: Woods, D.

Corporate Source: Univ of Surrey, Guildford, Engl

Conference Title: Colloquium on Advances in S-Parameter Measurement at Micro-Wavelengths.

Conference Location: London, Engl Conference Date: 19830523

Sponsor: IEE, Electronics Div, London, Engl

E.I. Conference No.: 04026

Source: IEE Colloquium (Digest) n 1983/53. Publ by IEE, London, Engl p 1. 1-1. 8

Publication Year: 1983

CODEN: DCILDN

Language: English

Document Type: PA; (Conference Paper)

Journal Announcement: 8508

Abstract: A 4-channel **bidirectional** network analyser (BNA) is a pair of 2-channel 4-port reflectometers operated alternately in active and passive modes in which the reflectometers individually measure S_{11} and S_{22} with the passive reflectometer acting as a substantially matched load to the unknown. Transmission parameters, S_{21} and S_{12} , are then obtained in terms of the ratio of the voltage response of the passive reflectometer to the reference voltage response of the active reflectometer. The reflectometers are symmetrical resistance-bridge networks. Vector-null detection is used, not only to improve the accuracy

of the voltage-ratio measurement but for the study of residual effects such as bad contacts, contact repeatability, cable flexing effects, stability, etc. No attempt is made to automate the system and **error correction** is carried out with an off-line computer. 8 refs.

10/7/14 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abstracts Online
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01613375 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
HIERARCHICAL AND INTEGRATED ERROR RECOVERY BASED ON BIDIRECTIONAL CHART PARSING TECHNIQUE

Author: MIN, KYONGHO

Degree: PH.D.

Year: 1997

Corporate Source/Institution: UNIVERSITY OF NEW SOUTH WALES (AUSTRALIA)
(0423)

Source: VOLUME 58/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 5488.

A system in this thesis employs a hierarchical error recovery strategy: a parser for well-formed sentences, a second parser for repairing single-error sentences, and a third parser for repairing multiple-error sentences. CHAPTER (CHART Parser for Two-stage Error Recovery) covers the first two stages, and MERCHANT (Multiple Error Recovery with CHARTs and Need-arc Trees) covers the third stage.

CHAPTER performs automatic syntactic and semantic parsing of ill-formed sentences, integrating various levels of information: lexical, syntactic, surface case, and semantic, using an augmented context-free grammar (augmented with syntactic feature constraints). It is composed of four layers of processes: morphological, syntactic, surface case, and semantic, and all subsystems are controlled by a single integrated-agenda system.

At the lexical level, for spelling **error correction**, the inferred syntactic information (i.e., syntactic category and features) and semantic information are used to reduce the number of alternative corrections; each correction also has a penalty score determined by a Pythagorean metric for the Qwerty keyboard layout. CHAPTER can use the semantic information to **correct real-word errors**, if a concept associated with the erroneous word violates semantic selectional restrictions.

At the syntactic level, for error recovery, the second parser employs generalised top-down chart parsing in **bidirectional** mode, and separates an **error correction** phase from an **error detection** phase. The best correction among alternative repairs is selected by heuristics (which are expressed in terms of penalty scores, based on error types and weight of a repaired constituent in a local tree).

Surface case processing maps a surface structure of a sentence to its deep structure using a transformational grammar model. The surface case processing aims to extract maximal syntactic information from the surface structure, to help interpret the meaning of the sentence. Semantic processing interprets the meaning of a sentence using semantic selectional restrictions: act templates based on a concept hierarchy and meta-concepts represented by a type of boolean expression. For ill-formed sentences, the semantic processing filters out meaningless repairs suggested by the syntactic recovery system.

10/7/15 (Item 2 from file: 35)

DIALOG(R)File 35:Dissertation Abstracts Online
(c) 1999 UMI. All rts. reserv.

01474989 ORDER NO: AADAA-I9611766
ROBUST CHECKSUM TEST IN ALGORITHM-BASED FAULT TOLERANCE ON 2-D PROCESSOR ARRAYS

Author: SONG, GI-YONG

Degree: PH.D.

Year: 1995

Corporate Source/Institution: UNIVERSITY OF SOUTHWESTERN LOUISIANA (0233

)

Director: JUNG H. KIM

Source: VOLUME 56/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 6873. 95 PAGES

Since the introduction of a system-level method for achieving fault tolerance called algorithm-based fault tolerance (ABFT) for array processors, a number of methods for the floating-point detection/correction problems have been proposed. Most ABFT schemes use a floating-point equality test to **detect errors** resulting from a hardware fault. But the limited precision of the contemporary machines makes the tests susceptible to roundoff inaccuracies in floating-point operations, causing either false alarm or undetected errors. The adoption of proper encoding schemes and the thresholding of the equality test have been commonly used to avoid these problems; however a good threshold is difficult to find, and these methods have not settled roundoff inaccuracies in floating-point operations perfectly.

When compared to the properly thresholded floating-point checksum test alone, the error coverage was greatly increased by the hybrid checksum test (AsDu92) which presented an integer-based equality test for checking in floating-point multiplication. But, the hybrid checksum test still counts on the threshold for checking in floating-point addition, so the number of **error detections** decreases with increases in dynamic range of input data.

The concurrent floating-point checksum test (CFPC) (WeiD93) was proposed for the error checking in floating-point addition without selecting proper threshold, providing a convincing error checking capability. This research was focused on the checking for the operations of mantissa part exclusively in the floating-point computation with the integer-based method.

In this dissertation, we propose a Modified Hybrid Checksum test (MHC), which consists of the Concurrent Floating-point Multiplication Checksum test and the Concurrent Floating-point Addition Checksum test. This scheme provides complete **error detection /correction** capabilities against any faults in the mantissa part of floating-point number as well as in the exponent part and normalization process of floating-point matrix-matrix multiplications, and locates the faulty processing element with less time latency and hardware overhead regardless of the dynamic range of input data. We apply the MHC test to the 2-D Unidirectional and **Bidirectional** arrays, which were proved to be most efficient in matrix-matrix multiplication, with fault-tolerance among related configurations (KiRe92), designing each required processing element and checking elements, and analyzing the hardware and time overhead.

10/7/16 (Item 3 from file: 35)

DIALOG(R)File 35:Dissertation Abstracts Online

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01449495 ORDER NO: AADAA-I9541493

A MONTE CARLO ASSESSMENT OF DFIT WITH POLYTOMOUSLY-SCORED UNIDIMENSIONAL TESTS (DIFFERENTIAL ITEM AND TEST FUNCTIONING, ITEM BIAS, TEST BIAS)

Author: FLOWERS, CLAUDIA PAISLEY

Degree: PH.D.

Year: 1995

Corporate Source/Institution: GEORGIA STATE UNIVERSITY (0079)

Source: VOLUME 56/08-A OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 3093. 116 PAGES

Statement of the problem. Differential item and test functioning (DIF and DTF) are statistical methods of detecting potentially biased items and tests. Raju, van der Linden, and Fleer (1992) proposed an IRT-based procedure, differential functioning of item and test (DFIT), for assessing DIF and DTF. The purpose of this study was to empirically assess the adequacy and validity of the DFIT framework using polytomously-scored data (i.e., test items that require more than correct/incorrect scoring).

Methods. Polytomous data for two test lengths (20 and 40 items) and

two Focal Group distributions ($N \sim (0,1)$ and $N \sim (-\$1,1)$) were simulated under conditions that varied in the number of DIF items (0%, 5%, 10%, and 20%), direction of DIF (unidirectional and balanced-**bidirectional**), and type of DIF (uniform and nonuniform).

Results. The findings provided empirical evidence that supported the theoretical expectations of the polytomous DFIT framework. The **detection errors** were low across all conditions.

Conclusions. The DFIT framework is a viable procedure for detecting differential functioning items and tests with polytomously-scored items for the conditions simulated. Limitations and future research are discussed.

10/7/17 (Item 4 from file: 35)

DIALOG(R)File 35:Dissertation Abstracts Online

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01369776 ORDER NO: AAD94-24208

MEXICO'S MACROECONOMIC PERFORMANCE: AN ANALYSIS USING CO-INTEGRATION TECHNIQUES

Author: DE LA CRUZ MARTINEZ, JUSTINO

Degree: PH.D.

Year: 1994

Corporate Source/Institution: IOWA STATE UNIVERSITY (0097)

Supervisor: WALTER ENDERS

Source: VOLUME 55/04-A OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 1053. 241 PAGES

In the context of the monetary approach to the balance of payments, co-integration and vector autoregressions techniques are applied to Mexican data. The statistical evidence suggests that, despite the presence of nonstationarity in Mexico's data, a long-run relationship seems to exist between changes in international reserves and the exchange rate and changes in domestic credit, i.e., these variables seem to be co-integrated. In addition, multivariate Granger causality tests together with innovation accounting support a negative **bidirectional** causality between these variables. This finding does not support the unidirectional causality of the monetary approach, or its assumption that domestic credit is exogenous. The **bidirectional** causality does indicate that Mexico's monetary authorities adjust domestic assets to sterilize exogenous balance-of-payments deficits on the monetary base in an attempt to control its monetary policy.

Moreover, co-integration and vector autoregressions techniques are again applied to Mexico's data to test whether purchasing power parity held during the period 1960-1988. The null hypothesis of non co-integration (e.g. purchasing power parity did not hold) was rejected in favor of accepting purchasing power parity. An estimated **error -correction** model suggests that Mexican prices and/or the peso price of a U.S. dollar adjusted as to maintain purchasing power parity during that period. This is also supported by innovation accounting and Granger causality tests derived from the estimated VAR.

Next, co-integration techniques are applied to Mexico's data to determine whether there exists statistical evidence of a long-run or equilibrium money demand specification during the period 1969 to 1991. Although three definitions of money supply were tested, only the monetary aggregate M3 seems to observe a long-run relationship with income and the rate of inflation. Further Chow tests detected a structural change in the money demand for M3 only after 1988.

10/7/18 (Item 1 from file: 103)

DIALOG(R)File 103:Energy SciTec

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03924189 GB-95-052612; EDB-96-007949

Title: Road transport energy demand in Australia. A cointegration approach

Author(s): Samimi, R.

Source: Energy Economics v 17:4. Coden: EECODR ISSN: 0140-9883

Publication Date: Oct 1995 p 329-339

Language: English

Abstract: A cointegration framework is used to examine the short-run and long-run characteristics of energy demand in the Australian road transport sector. A lagged endogenous equation based on a partial adjustment process is proposed and estimated. Results indicate that energy demand, output and real energy prices are integrated of order 1 and cointegrated. The long-run output and price elasticities of energy demand are estimated to be 0.52 and -0.12 respectively. Causality tests reveal a **bidirectional** causality path between output and energy demand and a unidirectional path from energy consumption to prices. No other causality paths between output, prices and energy demand are detected. The short-run output elasticity of energy demand is estimated to be 0.25 based on an **error-correction** model. The short-run price elasticity is found to be insignificant. The inertia parameter is 0.48 corresponding to 95% of the demand adjustment occurring after five periods. The results are compared with previous findings and the variations are partially attributed to the structural changes in the road transport sector in the 1980s, some of which are discussed.
(author)

10/7/19 (Item 2 from file: 103)

DIALOG(R)File 103:Energy SciTec

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03650278 EDB-94-066244

Title: Fault-tolerant corrector/detector chip for high-speed data processing

Author(s)/Editor(s): Andaleon, D.D.; Napolitano, L.M. Jr.; Redinbo, G.R.; Shreeve, W.O.

Patent No.: US 5291496 A

Patent Assignee(s): Dept. of Energy, Washington, DC ()

Priority No.: US 7-599606

Patent Date Filed: 18 Oct 1990

Publication Date: 1 Mar 1994 ([10] p)

Contract Number (DOE): AC04-76DP00789

Language: English

Availability: Patent and Trademark Office, Box 9, Washington, DC 20232
(United States)

Abstract: An internally fault-tolerant data **error detection** and **correction** integrated circuit device and a method of operating same is described. The device functions as a **bidirectional** data buffer between a 32-bit data processor and the remainder of a data processing system and provides a 32-bit datum with a relatively short eight bits of data-protecting parity. The 32-bits of data by eight bits of parity is partitioned into eight 4-bit nibbles and two 4-bit nibbles, respectively. For data flowing towards the processor the data and parity nibbles are checked in parallel and in a single operation employing a dual orthogonal basis technique. The dual orthogonal basis increase the efficiency of the implementation. Any one of ten (eight data, two parity) nibbles are correctable if erroneous, or two different erroneous nibbles are detectable. For data flowing away from the processor the appropriate parity nibble values are calculated and transmitted to the system along with the data. The device regenerates parity values for data flowing in either direction and compares regenerated to generated parity with a totally self-checking equality checker. As such, the device is self-validating and enabled to both detect and indicate an occurrence of an internal failure. A generalization of the device to protect 64-bit data with 16-bit parity to protect against byte-wide errors is also presented. 8 figures.

10/7/20 (Item 3 from file: 103)

DIALOG(R)File 103:Energy SciTec

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03469798 NOV-93-011024; EDB-93-048674

Title: Novel circuits for radiation hardened memories

Author(s): Haraszti, T.P.; Mento, R.P. (Microcirc Associates, Newport Beach, CA (United States)); Moyer, N.E. (Hughes Aircraft (United States)); Grant, W.M. (AMI-Gould (United States))
Conference Title: 1991 Institute of Electrical and Electronic Engineers (IEEE) nuclear science symposium and medical imaging conference
Conference Location: Santa Fe, NM (United States) Conference Date: 2-9 Nov 1991
Source: IEEE Transactions on Nuclear Science (Institute of Electrical and Electronics Engineers) (United States) v 39:5. Coden: IETNAE ISSN: 0018-9499

Publication Date: Oct 1992 p 1341-1351

Report Number(s): CONF-911106--

Language: English

Abstract: This paper reports on implementation of large storage semiconductor memories which combine radiation hardness with high packing density, operational speed, and low power dissipation and require both hardened circuit and hardened process technologies. Novel circuits, including orthogonal shuffle type of write-read arrays, **error correction** by weighted **bidirectional** codes and associative iterative repair circuits, are proposed for significant improvements of SRAMs' immunity against the effects of total dose and cosmic particle impacts. The implementation of the proposed circuit resulted in fault-tolerant 40-Mbit and 10-Mbit monolithic memories featuring a data rate of 120 MHz and power dissipation of 880 mW. These experimental serial-parallel memories were fabricated with a nonhardened standard CMOS processing technology, yet provided a total dose hardness of 1 Mrad and a projected SEU rate of 1 [times] 10^{[minus] 12} error/bit/day. Using radiation hardened processing improvements by factors of 10 to 100 are predicted in both total dose hardness and SEU rate.

10/7/21 (Item 1 from file: 202)

DIALOG(R)File 202:Information Science Abs.

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00157779 9107779

ISA Document Number in Printed Publication: 9108104

Upper bounds on error-correcting runlength-limited block codes.

Document Type: Journal Article

Author (Affiliation): Hrehus, O.

Journal: IEEE Transactions on Information Theory

Publication Language(s): English

Source: Vol. 37 Issue 2 p. 941-945 May 1991 14

This paper derives some upper bounds on the size of a constrained, simple-**error correcting** block code. Two **directions** in which the codes are extended are studied: to **error-correcting** trellis codes, and to more complex **error-correcting** schemes. The paper focuses on simple **error-correcting** schemes, discusses the notion of a (d,k)-constrained block code, and introduces the concept of combined codes. Some bounds are derived. Examples are provided.

10/7/22 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

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5169010 INSPEC Abstract Number: C9603-4210L-009

Title: Parsing ill-formed input as A* search using generalized edges

Author(s): Kato, T.

Author Affiliation: NTT Inf. & Commun. Syst. Lab., Japan

Journal: Transactions of the Information Processing Society of Japan

vol.36, no.10 p.2343-52

Publisher: Inf. Process. Soc. Japan,

Publication Date: Oct. 1995 Country of Publication: Japan

CODEN: JSGRD5 ISSN: 0387-5806

SICI: 0387-5806(199510)36:10L:2343:PFIS;1-Y

Material Identity Number: T205-96001

Language: Japanese Document Type: Journal Paper (JP)

Treatment: Theoretical (T)

Abstract: A chart based technique for parsing ill formed input is proposed. This can process sentences with unknown/misspelled words, omitted words or extraneous words. This generalized parsing strategy is, similar to C.S. Mellish's (1989), based on an active chart parser, and shares the many advantages of Mellish's technique. It is based on pure syntactics, it is independent of all grammars, and it does not slow down the original parsing operation if there is no ill formedness. However, unlike Mellish's technique, it doesn't employ any complicated heuristic parameters. There are two key points. First, instead of using a unified or interleaved process for finding **errors** and **correcting** them, we separate the initial **error detection** stage from the other stages and adopt a version of **bidirectional** parsing. This effectively prunes the search space. Second, it employs normal top down parsing, in which each parsing state reflects the global context, instead of top down chart parsing. This enables the technique to determine the global plausibility of candidates easily, based on an admissible A* search. The proposed strategy could enumerate all possible minimal penalty solutions in just 4 times the time taken to parse the correct sentences. (23 Refs)

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10/7/23 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

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4518616 INSPEC Abstract Number: B9312-1265B-118, C9312-5210-038

Title: **Modular-addition signature analysis for built-in self-test**

Author(s): Cheng-Wen Wu; Hun-Song Chen

Author Affiliation: Dept. of Electr. Eng., Nat. Tsing Hua Univ., Hsinchu, Taiwan

Conference Title: Proceedings of ETC 93. Third European Test Conference (Cat. No.93TH0494-5) p.457-65

Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA

Publication Date: 1993 Country of Publication: USA xvi+548 pp.

ISBN: 0 8186 3360 3

U.S. Copyright Clearance Center Code: 0 8186 3360 3/93/\$3.00

Conference Sponsor: IEEE; EUREL

Conference Date: 19-22 April 1993 Conference Location: Rotterdam, Netherlands

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: The conventional multiple input signature register (MISR) has an average time to alias of $2^n/n$ (n is the length of the register), i.e., its aliasing probability is $1/2^n$. This paper presents a new cellular-automaton structure called modular-addition signature analyzer (MASA), which is shown to be an excellent alternative of MISR. It has a much lower hardware overhead than MISR based on equal aliasing probability. Experimental results show that, for $n=16$, MASA uses no more than 60% of the silicon area which MISR requires. The authors evaluate its ECs with respect to various error models, which shows consistently high ECs even for multiple errors. Its error coverages are easier to analyze than those of MISR. It can **detect** all single **errors**, multiple output stuck faults, and most of the unidirectional and **bidirectional** errors. In general, any error on a CUT output stream which makes the number of 1s (modulo 4) being different from N (modulo 4) is detectable by MASA at a CUT output, where N is the correct number of 1s at the CUT output stream. (18 Refs)

10/7/24 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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04117827 INSPEC Abstract Number: B9205-8110B-022, C9205-3340H-018

Title: **High voltage under-ground cable data communications for high speed unit protection and control**

Author(s): Redfern, M.A.; Bo, Z.; Ormondroyd, R.F.; McGuinness, P.; Yip,

H.T.

Author Affiliation: Bath Univ., UK

Conference Title: APSCOM-91. 1991 International Conference on Advances in Power System Control, Operation and Management (Conf. Publ. No.348) p. 244-9 vol.1

Publisher: IEE, Hong Kong

Publication Date: 1991 Country of Publication: Hong Kong 2 vol. xvii+932 pp.

ISBN: 0 86341 246 7

Conference Date: 5-8 Nov. 1991 Conference Location: Hong Kong

Availability: IEE, London, UK

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: The authors present the findings of an on-going investigation into the use of HV power cables for high security, dedicated data communications between substations. This communications system provides the data transfer required for high speed unit protection of distribution feeder circuits and network automation. The communications system uses a high frequency carrier with the line driver and receiver circuits tuned to pre-defined channels. The propagation characteristics of typical underground HV cables together with the coupling circuits have been examined. The internal protocols and coding techniques used to organise the data into message blocks and to provide **error detection** and limited **correction** are introduced. Using 80 kBits/sec **bi-directional** data transmission along the power circuit, the system provides user data rates of 40.8 kbits/sec for protection and 4.8 kbits/sec for network automation and 4.8 kbits/sec for 'house-keeping'. (10 Refs)

10/7/25 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

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03770966 INSPEC Abstract Number: B90080552, C90068682

Title: ROBCOM: new bidirectional centralised remote control system for distribution networks

Author(s): Huysmans, V.

Journal: Revue E vol.106, no.2 p.22-5

Publication Date: 1990 Country of Publication: Belgium

CODEN: RBBEA9 ISSN: 0770-0024

Language: French Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P)

Abstract: The characteristics of distribution networks are analysed in depth at the level of high-frequency signal transmission. A system adapted to such a channel is developed on the principle of very wideband data packet transmission in blocks with frequency hopping, for synchronisation at the receiver. **Error detection** and **correction** codes and a network protocol based on the OSI seven-layer model are described. The system is compared with a conventional narrowband uncoded system on the basis of message residual error rate, and shows a 20 dB advantage. Trial results from the Swiss low- and medium-voltage networks are reported. An application to remote meter reading is illustrated. (0 Refs)

10/7/26 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

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03465469 INSPEC Abstract Number: C89061900

Title: Bidirectional buffering speeds RISC-to-SCSI communication

Author(s): Eidson, S.; Lengoc, D.; Lin, J.

Author Affiliation: Integrated Device Technol. Inc., Santa Clara, CA, USA

Journal: Electronic Design vol.37, no.15 p.67-70, 72, 74

Publication Date: 13 July 1989 Country of Publication: USA

CODEN: ELODAW ISSN: 0013-4872

Language: English Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P)

Abstract: Discusses two-way buffering that matches the 32-bit RISC bus to

the 8-bit peripheral channel. The authors describe a system incorporating a R3000 RISC microprocessor and a 5380 SCSI controller can be divided into three major blocks: the processor, the memory interface, and the peripheral controller. The processor-to-peripheral interface is complicated. First, data transfers between components of different speeds can drastically reduce throughput. Even with a direct-memory-access channel between the processor and peripheral, the processor must be ready to relinquish the bus on short notice and go to an idle condition. In addition, the data reduction from a 32- to an 8-bit bus is like a funnel that can drop performance by a factor of four. To keep the data flow at or near the level of a RISC processor, data folding and sophisticated buffering are necessary. Finally, data integrity is important, and **error detection** and/or **correction** should be incorporated into any peripheral channel. (0 Refs)

10/7/27 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

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03170655 INSPEC Abstract Number: B88047403, C88039171

Title: Modular workstation

Author(s): Spundflasche, R.

Author Affiliation: Transtech GmbH, Heilbronn, West Germany

Journal: Elektronik Industrie vol.19, no.2 p.24, 26-7

Publication Date: 1988 Country of Publication: West Germany

CODEN: EKIDAT ISSN: 0374-3144

Language: German Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P)

Abstract: Describes the principles, construction and application of the 'Measurement and Computation Tools Workstation' of EIP Microwave of CA, USA. It intends to eliminate the task of building up a test station for automatic testing from a multitude of incompatible instruments. It comprises a hardware module containing signal generators, amplifiers, A/D converters, detectors, etc., and a software module for data acquisition, **error correction**, input/output. An example illustrates its use as a **bi-directional** vectorial network analyser in the 1 to 18 GHz frequency range. In this configuration it contains an IBM PC AT, high-resolution monitor, frequency synthesizer, A/D converter, multi-channel IF amplifier and power supplies, as well as a 68020 processor with two floating-point coprocessors.

10/7/28 (Item 7 from file: 2)

DIALOG(R)File 2:INSPEC

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03052573 INSPEC Abstract Number: B88006838, C88007524

Title: Selector-line merged built-in ECC technique for DRAMs

Author(s): Yamada, J.

Author Affiliation: NTT Corp., Kanagawa, Japan

Journal: IEEE Journal of Solid-State Circuits vol.SC-22, no.5 p.

868-73

Publication Date: Oct. 1987 Country of Publication: USA

CODEN: IJSCBC ISSN: 0018-9200

U.S. Copyright Clearance Center Code: 0018-9200/87/1000-0868\$01.00

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: A high-performance built-in **error** checking and **correcting** (ECC) technique applicable to megabit-level dynamic RAM (DRAM) chips is described. This technique, based on a **bidirectional** parity code, achieves high-speed **error correction** with a minimum increase in area. The impact of the technique on access time and chip overhead is discussed. Furthermore, effects on soft-error reduction and yield improvement are analytically investigated. (6 Refs)

10/7/29 (Item 8 from file: 2)

DIALOG(R)File 2:INSPEC

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02819685 INSPEC Abstract Number: A87014989, B87014577, C87012945

Title: A system for fast measurement of optical gain in discharges

Author(s): Roll, G.; Mentel, J.

Author Affiliation: Allgemeine Elektrotech. und Elektrooptik, Ruhr-Univ., Bochum, West Germany

Journal: Journal of Physics E (Scientific Instruments) vol.19, no.9
p.718-21

Publication Date: Sept. 1986 Country of Publication: UK

CODEN: JPSIAE ISSN: 0022-3735

U.S. Copyright Clearance Center Code: 0022-3735/86/090718+04\$02.50

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: The measurement of optical gain by means of measuring the amplification of the spontaneous emission is based on a relatively simple principle. A feedback optical system reflects emitted light back into the discharge where it may be amplified or absorbed. A new all-purpose system is described which is independent of the discharge geometry and which determines the gain from simultaneous measurements in **two directions** of polarisation. Charge-coupled devices (CCDS) are employed as optical detectors. The system records a spectral range of about 20 nm simultaneously. The special features of the CCDS permit the realisation of a fast optical shutter. A microprocessor system is used for controlling the measurement, evaluating the measured data and **correcting errors** due to the optical set-up. (7 Refs)

10/7/30 (Item 9 from file: 2)

DIALOG(R)File 2:INSPEC

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02694392 INSPEC Abstract Number: B86041117, C86033982

Title: A multi-bit-wide dynamic RAM with a built-in ECC circuit

Author(s): Yamada, J.; Date, S.; Mano, T.

Author Affiliation: NTT Electr. Commun. Labs., Atsugi-Shi, Japan

Journal: Transactions of the Institute of Electronics and Communication Engineers of Japan, Part C vol.J69C, no.1 p.9-16

Publication Date: Jan. 1986 Country of Publication: Japan

CODEN: DTGCAY ISSN: 0373-6113

Language: Japanese Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: A built-in **error** checking and **correcting** (ECC) circuit applicable to a wide variety of word organizations in megabit level dynamic RAMs is required to reduce alpha particle-induced soft error rates. The authors describe a new ECC method to check and correct a plurality of readout data at one time using a **bi-directional** parity code. A memory configuration by which a small-sized ECC circuit may be realized is also proposed. Moreover, a 4 bit-at-a-time built-in ECC circuit was applied to a 1 Mbit dynamic RAM, achieving a sufficiently low soft error rate with a low chip overhead of 12% and a measured **error correcting** time of 20 ns. (8 Refs)

10/7/31 (Item 10 from file: 2)

DIALOG(R)File 2:INSPEC

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02408590 INSPEC Abstract Number: B85017419, C85014856

Title: Built-in ECC techniques for LSI memories

Author(s): Yamada, J.; Mano, T.; Date, S.

Author Affiliation: Atsugi Electr. Commun. Lab., NTT, Japan

Journal: Transactions of the Institute of Electronics and Communication Engineers of Japan, Part C vol.J67C, no.10 p.777-84

Publication Date: Oct. 1984 Country of Publication: Japan

CODEN: DTGCAY ISSN: 0373-6113

Language: Japanese Document Type: Journal Paper (JP)

· Treatment: Applications (A); Practical (P)

Abstract: A built-in **Error** Checking and **Correcting** (ECC) is essential for megabit level dynamic RAMs to reduce an alpha particle-induced soft error rate. The authors propose some of the new built-in ECC techniques. The advantages and disadvantages of these techniques are also discussed in relation to memory overhead, **error correcting** time, and the soft error rate. Consequently, it is shown that an ECC method using a **bidirectional** parity code is best suited for a built-in ECC applicable to megabit level dynamic RAMs. (8 Refs)

10/7/32 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

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01173291 JICST ACCESSION NUMBER: 90A0694523 FILE SEGMENT: JICST-E

Theory and construction of unidirectional byte error correcting codes.

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Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report
(Institute of Electronics, Information and Communication Engineers),
1990 , VOL.90,NO.152(IT90 33-51), PAGE.25-30, FIG.2, TBL.3, REF.14

JOURNAL NUMBER: S0532BBG

UNIVERSAL DECIMAL CLASSIFICATION: 621.391.037.3

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: Codes **correcting /detecting** unidirectional byte **errors** are investigated. It is shown that such codes have the capability of correcting combinations of **bidirectional** and unidirectional byte errors. This paper also gives a code construction. This is derived from combination of two codes. The one is a code for encoding the Hamming weights of data bytes and used to estimate error-locations. The other is a byte-**error -correcting** code for **error -evaluation**. Moreover, we describe a decoding procedure of the codes correcting combinations of **bidirectional** and unidirectional byte errors. (author abst.)

10/7/33 (Item 1 from file: 6)

DIALOG(R)File 6:NTIS

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1294122 NTIS Accession Number: DE87750810

Satellite Measurements of the Radiation Budget: Random Sampling Test and Recovery of the Radiation Flux Density

Stuhlmann, R.

Cologne Univ. (Germany, F.R.). Inst. of Geophysics and Meteorology.

Corp. Source Codes: 006650007; 9201825

Report No.: NP-7750810

1985 85p

Languages: German

Journal Announcement: GRAI8712; NSA1200

In German. Mitteilungen aus dem Institut fuer Geophysik und Meteorologie der Universitaet zu Koeln. No. 47.

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NTIS Prices: MF A01

Country of Publication: Germany, Federal Republic of

First the sampling of 2-D signals by Narrow Field Of View (NFOV) radiometers is discussed. Therefore it is assumed that the statistical properties of the radiance field can be estimated by a Markov-random process. By means of Fourier-transformation 'blurring' is defined by the ratio of power of the measured signal and that of the radiance field, where it is assumed that no aliasing noise and no noise introduced by the side

bands of the modulation transfer function are present. Thus if the ratio of blurring is equal to one all information about the spatial structure in the radiance field is contained by the recorded signal. It is shown that this ratio reaches the value of 0.95 when the mean width of spatial structure in the radiance field is about ten times larger than the FOV of the instrument. The second part of the study is concerned with the retrieval of broad band exitances from the recorded radiances. Therefore narrow to broad band filter corrections as well as **bidirectional** reflectance functions are calculated by radiative transfer calculations. (ERA citation 12:009888)

10/7/34 (Item 1 from file: 144)
DIALOG(R) File 144:Pascal
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13225332 PASCAL No.: 97-0492787
Descriptive analysis of voice, data and image flows : basic concepts
Analyse descriptive des flux voix, donnees et image : notions de base
FOUQUET Y; SANCHEZ P; VIDRASCU A
Electricite de France. Direction des etudes et recherches, Clamart, France; Electricite de France. Departement ingenierie de la communication en informatique, Clamart, France
Journal: Collection de notes internes de la Direction des etudes et recherches. Mathematiques, informatique, telecommunications, 1997 (33) 16 p., tabl., fig. Non-paginated pages/foldouts
ISSN: 1161-059X Availability: INIST-26165 F; 354000068713140000
Report No.: EDF-DER 297-NJ-00033
Document Type: P (Serial); R (Report) ; M (Monographic)
Country of Publication: France
Language: French Summary Language: French; English
The characteristics of voice, data and image flows are different and the constraints linked to them generally require different physical infrastructures. Therefore items which can characterize voice transportation are as follows : - real time (if **bidirectional**) ; - constant traffic (if voice digitised, PABX example) ; - fixed transmission block lengths ; - time constraints do not authorize simple **error detection** , only **corrections** can be considered (correcting codes). So the system used shall be reliable ; - no flow control. Items which can characterize data transmission are : - real time or not ; - random type traffic profile (by bursts or uniform) ; - transmission block lengths ; - **error correction** capability ; - possible flow control (pass band and quality adaptation available). Lastly items which can characterize images are as follows : - real time (if **bidirectional**) ; - variable traffic, transaction feature (except when the fixed H221 frame is used) ; - time constraints do not authorize simple **error detection** , only **corrections** can be considered (correcting codes). So the system used shall be reliable ; - no flow control. Development of digital techniques has however enabled telephony and multiplexing techniques to be developed. As a result, "voice-data" integration on the same support offers minimization of network infrastructure costs. On its side, the image benefited from compression techniques to generate the multimedia which groups the three flows together. The quantities of information to be exchanged are becoming greater and the infrastructure constraints more numerous. "Voice - Data - Images" integration should be widely developed, particularly in the field of extended networks (WAN) thanks to optimization of costs which it may bear, and in the field of local networks (LAN) with the arrival of multimedia kits for PCs or UNIX stations at very attractive prices.
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10/7/35 (Item 2 from file: 144)
DIALOG(R) File 144:Pascal
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12595698 PASCAL No.: 96-0282730
Useful evidence on negative evidence
BOHANNON J N III; PADGETT R J; NELSON K E; MARK M
Butler University, United States

Journal: Developmental psychology, 1996 , 32 (3) 551-555
ISSN: 0012-1649 CODEN: DEVPA9 Availability: INIST-17069;
354000043720000170

No. of Refs.: 23 ref.

Document Type: P (Serial) ; A (Analytic)

Country of Publication: United States

Language: English

J. L. Morgan, K. M. Bonamo, and L. L. Travis (1995) applied synchronous and time-series regression techniques to observational data to **detect** effects of recasted **error correction** on children's emerging grammar. Results showed that recasts did not facilitate learning but actually impeded it. In this study, a formal modeling procedure was used to generate similar time series with known, underlying learning relations. The regression procedures used by Morgan et al. could not discriminate between the data generated by models in which recasts (a) totally determined grammatical learning, (b) supplemented other learning, (c) inhibited learning, or (d) had nothing to do with grammatical learning. These modeling results and review of statistical and conceptual problems indicate that Morgan et al.'s analyses (short term as well as long term) are uninterpretable as regards the role of recasts or any form of negative evidence in children's syntactic acquisition. However, their descriptive data confirm many prior reports on when parents use recasts and raise interesting questions about possible **bidirectional** influences between adult recasts of a syntactic structure and the acquisition of that structure.

10/7/36 (Item 3 from file: 144)

DIALOG(R)File 144:Pascal

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12374214 PASCAL No.: 96-0020253

The development of children adopted for romanian orphanages

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Journal: Merrill-Palmer quarterly : (1960), 1995 , 41 (4) 411-430

ISSN: 0272-930X Availability: INIST-21596; 354000058932280010

No. of Refs.: 1 p.1/4

Document Type: P (Serial) ; A (Analytic)

Country of Publication: USA

Language: English

A cointegration framework is used to examine the short-run and long-run characteristics of energy demand in the Australian road transport sector. A lagged endogenous equation based on a partial adjustment process is proposed and estimated. Results indicate that energy demand, output and real energy prices are integrated of order 1 and cointegrated. The long-run output and price elasticities of energy demand are estimated to be 0.52 and -0.12 respectively. Causality tests reveal a **bidirectional** causality path between output and energy demand and a unidirectional path from energy consumption to prices. No other causality paths between output, prices and energy demand are detected. The short-run output elasticity of energy demand is estimated to be 0.25 based on an **error -correction** model. The short-run price elasticity is found to be insignificant. The inertia parameter is 0.48 corresponding to 95% of the demand adjustment occurring after five periods. The results are compared with previous findings and the variations are partially attributed to the structural changes in the road transport sector in the 1980s, some of which are discussed.

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